Most Significant Bits

Intel P6, AMD K5 Hit First Silicon

Accelerating into the next generation, Intel's P6 processor achieved first silicon in October. The company is currently verifying the functions of the device, which it hopes to sample as early as 1Q95. It now appears that P6 system shipments could begin in 3Q95 rather than toward the end of next year, as previously expected. The initial focus of P6 will be on servers, although the chip will appear in some high-end desktops as well.

Intel released no new information about the P6 design, which will be unveiled at ISSCC in February. We expect the processor to issue three or four instructions per cycle and include many of the advanced features of AMD's K5 design *(see **081401.PDF**)*, such as register renaming and speculative and out-of-order execution. The clock rate will probably be 133 or 150 MHz, with SPECint92 performance of about 200, twice that of the current high-end Pentium and significantly better than the K5's projected performance.

Coincidentally, the K5 reached first silicon in mid-November, just a few weeks after the P6. Both these chips, as well as Cyrix's Pentium-class M1 *(see **081601.PDF**)*, appear to be on about the same schedule, putting Intel one full generation ahead of its major competitors.

Digital, Mitsubishi Push 21066 to 233 MHz

At Comdex, Digital announced a 0.5-micron version of its highly integrated 21066 processor that increases the clock speed by 40% over the previous version. The new 21066A operates at 233 MHz and delivers 94 SPECint92 and 110 SPECfp92 in Digital's evaluation board. The company has not announced a system using the 233-MHz chip, although it did finally announce a 166-MHz 21066 system.

Other than clock speed, the 21066A is functionally identical to the original design, which includes cache, DRAM, and PCI interfaces. One exception is that the new design includes a sleep mode for power management, which simply divides the input clock by 2, 4, or 8. Maximum power at 233 MHz is 23 W, the same as a 166-MHz 21066, but in sleep mode it drops as low as 3 W, still well beyond the acceptable range for portable systems.

The 0.5-micron process reduces the die size of the new part by 23%, to 161 mm^2. This in turn cuts the estimated manufacturing cost by about 20%, to $125, according to the MPR Cost Model *(see **081203.PDF**)*. The 21066A is priced at $396 in quantities of 1,000, just $14 more than the 21066. It is currently sampling and due to begin volume shipments in 1Q95.

Mitsubishi, which had previously announced a 200-MHz 21066 *(see **0813MSB.PDF**)*, said that it will match the 233-MHz speed grade but not Digital's prices. Mitsubishi will sell the part for $490 in quantities of 1,000 and does not plan volume deliveries until 3Q95, casting doubt on its seriousness about the Alpha market.

The process shrink increases the attractiveness of the 21066 for NT systems. At 233 MHz, it should deliver similar performance to a 90-MHz Pentium at about 60% of the cost of a Pentium processor with a system-logic chip set comparable to the Alpha chip's features. The 21066 is just the entry point to the Alpha line, which offers performance of up to 200 SPECint92 today and more than 300 SPECint92 next quarter. Digital claims that more than 750 software applications are shipping for NT-on-Alpha, with nearly 700 more in the pipe.

Digital will also use the 21066A to upgrade its embedded product line, which currently consists of the 66-MHz 21068. The company will offer a 100-MHz version of the 21066A for just $193 in quantities of 1,000. At this speed, the processor dissipates 10 W. A company called Prime Option will use the new chip in a high-end printer, but even at $193, the Alpha processor is too expensive and power-hungry for all but the highest-priced embedded products.

SPEC Changes Rules, Results Inflate

In a clarification of its existing run rules, the SPEC committee now allows vendors to direct the output of the 072.sc benchmark to disk rather than the screen, eliminating the impact of vendor-specific "curses" packages. Some vendors had already been writing to a file, but many had not. This clarification levels the playing field.

This small change makes a big difference, however. Intel has reported new measurements for Pentium that show a 92% increase in the score for 072.sc. This increase alone is enough to boost Pentium's SPECint92 rating by about 12%. With the new rules, a 100-MHz Pentium is now rated at 113 SPECint92. The 60-MHz chip now reaches 70 SPECint92.

Also taking advantage of the change, Silicon Graphics increased its SPECint92 estimates for the 200-MHz R4400 from 130 to 141. Digital has measured 200 SPECint92 on its 275-MHz 21064A system, up from 189. These sorts of changes will ripple through the rest of the industry before things settle down.

Although SPEC saw no other feasible way to resolve the inconsistencies in 072.sc results, the new rules inflate the results of this component to typically twice the SPECint92 score, causing a repeat of the matrix300 phenomenon. When new preprocessor techniques sent matrix300 scores soaring a few years ago, it was difficult to compare SPEC scores between vendors using the latest techniques and those that were not. This situation ultimately caused the demise of the SPEC89 suite. We

can only hope that SPEC95 will appear soon and save us from this morass.

Intel Fixes Pentium FPU Bug

Despite exhaustive testing, a minor bug exists in many of the Pentium chips that Intel has shipped. The bug causes certain divisors to generate incorrect results beyond the eighth decimal place. For example, the floating-point calculation (1 ÷ 824633702441) produces:

$1.21265962940867 \times 10^{-12}$ on a Pentium;

$1.21265962489116 \times 10^{-12}$ is the correct answer.

An Internet posting from mathematician Andreas Kaiser lists 23 divisors that produce similarly incorrect results, out of the 25 billion that he tested.

Intel has confirmed the error, which is caused by a bug in the floating-point state machine that controls the iterative divide process. All failing divisors have a similar binary pattern, which apparently causes the state machine to generate incorrect results after the first several iterations. Intel fixed the bug with a metal-mask change; currently shipping parts use the new masks. Unlike Cyrix, which fixed a similarly obscure bug in its 486 FPU *(see **080703.PDF**)*, Intel has offered to replace the processor of any user affected by the problem.

This offer should not have many takers, as the few divisors that generate erroneous results cause errors of a few parts per billion. Single-precision calculations are not affected at all. Most PC users don't even use their FPU, and engineers typically use single-precision.

The error does affect scientists and mathematicians who perform double-precision calculations. This community, though small, is outraged about the problem, which leaves in doubt any such technical work done on a Pentium system. Intel compounded the problem by not publicizing the bug when the company discovered it last summer and by not relabeling the corrected parts.

Intel had hoped that Pentium would expand its presence in the realm of scientific computing, which has been dominated by faster RISC processors. This bug, and Intel's crude attempt to cover it up, will jeopardize that effort, at least temporarily.

Opti Viper Supports Pentium-Class CPUs

Opti has introduced a PCI-based system-logic chip set designed to support both 5-V and 3.3-V Pentium processors, as well as Cyrix's M1 and AMD's K5. The chip set is designed to give system makers the flexibility to use a variety of processors in one motherboard design; in the past, different chip sets have been required for P5 and P54C Pentiums. PicoPower's new Golden Gate chip set offers a similar set of features.

The Viper chip set also includes special features to support non-Intel processors, allowing the system vendor to keep its options open. For example, Viper supports the linear burst mode used by Cyrix's M1 *(see **081601.PDF**)*. Opti claims that the chip set will support bus rates of up to 80 MHz, allowing for the possibility of a 150-MHz processor operating with a 2× clock multiplier instead of the expected 3×.

Opti claims that its highly tuned cache and DRAM systems deliver 5–10% better performance than competing chip sets. The design supports conventional or EDO DRAM and either conventional, synchronous, or pipelined burst SRAM for the cache. The cache can also be omitted, an option that may be attractive as Pentium systems push further down into the mainstream.

The chip set includes Intel's I/O APIC, supporting Intel's glueless dual-processor design for P54C systems. Opti chose not to include the alternative multiprocessor support logic for the AMD or Cyrix schemes, which appear to still be in flux, but they can be supported with a simple external gate array.

The three-chip set—which includes a PQFP-208 peripheral controller, a PQFP-208 system controller, and a PQFP-160 data buffer—is priced at $30 in OEM quantities. Samples are available now, with production in December. A fourth chip, a PCI-IDE controller that offers SCSI-like performance features with low-cost IDE drives, costs $5 and is now in production.

Errata: National 32000

In our article on National's Piranha *(see **081502.PDF**)*, we incorrectly described National's position in the embedded-processor market. National is a major player in the market for low-cost (8- and 16-bit) embedded processors. In addition, the company continues to sell its 32000 family of 32-bit embedded processors, although these devices will probably be superseded over time by new Piranha chips. ♦

