Most Significant Bits

Intel Delays Pentium "Announcement"

In yet another shift in the Pentium roll-out plan, Intel has decided to call the next batch of revelations—scheduled for March 22—a technology disclosure and not an announcement. Intel says that production (B-1 stepping) chips will be shipping at the time of the "disclosure." The only detail that will be held until the "announcement," now scheduled for May 20, is the price.

Intel insists that there has been no delay in the planned production ramp. Initial quantities will be small, however; Intel has told its customers that it expects to ship a total of 10,000 chips in 2Q93.

Intel sources say that the change was made under heavy pressure from a few major system makers, which were concerned that they wouldn't have enough chips by March 22 to meet the demand for systems. The pressure apparently comes from some large Intel customers that won't announce systems until they have substantial inventory. These system vendors don't want to be scooped by other companies that are willing to announce systems when they have only a handful of chips.

Intel will keep system makers bound by non-disclosure agreements until May 20, keeping them from announcing systems before that date. (Should any vendor consider ignoring Intel's "request," Intel's memo to the system vendors makes the consequences clear: chip shipments will be cut off.) While this will appease a few big companies, it will wreak havoc with the plans of many other system vendors. In effect, Intel is forcing all its customers to follow the announcement strategy of a few large, conservative system makers that are probably worried about hurting demand for high-end 486 systems.

R4400 Delivers Impressive Benchmarks

Silicon Graphics announced several new systems using its new R4400 processor *(see **070202.PDF**)*. These announcements provided the first measured benchmarks of the R4400 *(see **061503.PDF**)*. The Indigo^2 system, using a 150-MHz R4400, is quoted at 82 SPECint92 and 86 SPECfp92. The R4400 version of the new system will be available in 3Q93 at a base price of $20,500.

The SPEC92 results provide less improvement over the R4000 than the 60% gain seen in simulated SPEC89 values, but the integer performance exceeds that of all workstations shipping today. Only the fastest DEC Alpha chips, which are available exclusively in expensive server systems, can top the R4400 in integer performance. On the floating-point side, the new MIPS chip still significantly lags chips from DEC, HP, and IBM.

Like the 21064, the R4400 initially will be available only in the high-end servers as the chip vendors begin ramping up production in March. Full production volumes of the new chip are expected around mid-year, in time for system shipments in the third quarter. Faster desktop systems from DEC and IBM in that timeframe may prevent SGI from gaining the performance lead.

IBM Provides First Details of RIOS 2

For the past three years, IBM has tweaked and shrunk its original RIOS (RS/6000) chip set through three IC processes, scaling the clock rate from 25 to 62.5 MHz and enlarging the instruction cache size from 8K to 32K. IBM recently disclosed information on a brand-new design that extends the capabilities of RIOS 1.

RIOS 2 will be a three-chip design using about the same partitioning as its predecessor. To take advantage of the added real estate on the computational chips, the FXU (integer) and FPU chips will each have two complete functional units. Although the RIOS 1 design could issue two instructions to the FXU or FPU in a single cycle, the new chips can actually execute two instructions per cycle. The new instruction unit can issue up to six instructions on each cycle: two integer, two FP, one branch, and one condition.

The data cache chips probably will be expanded to allow cache sizes up to 256K. IBM promises that new features will be used to improve on the already-formidable memory bandwidth of RIOS 1, but did not offer more specifics. To increase the clock rate beyond the current 62.5 MHz, the entire chip set—three processor chips, four cache chips, and two system chips—will be packaged in a multichip module (MCM).

The company would not offer any specific clock speed or performance targets. Because RIOS 2 will use the same 0.7-micron technology as RIOS 1 uses today, the clock rate improvement will come primarily from the MCM technology; based on typical gains from MCMs, this should boost RIOS 2 into the 80–100 MHz range. This clock rate and the dual integer units should boost SPECint92 to around 100, re-establishing IBM as the performance leader. FP performance could reach 250 SPECfp92, exceeding even SGI's forthcoming TFP.

The first system shipments using RIOS 2 are expected around 3Q93. The new chip set was developed wholly by IBM, and the company does not plan to make it available on the open market.

IBM also admitted that it has added a little-endian switch to the PowerPC 601 on the second revision of the chip. This allows Intel-based operating systems such as Windows NT to be easily ported to the new processor. Bill Filip, head of IBM's RS/6000 business, said that IBM has no plans to sell NT-based PowerPC systems, but would welcome Microsoft or any other third party that wanted to port NT to PowerPC. Sun's Scott McNealy was recently

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quoted as offering a similar invitation to third parties, but SPARC now stands alone as the only RISC architecture without a little-endian offering.

Motorola (Finally) Announces the 88110

More than two years after it first revealed its 88000 follow-on, Motorola said that the 88110 is now in production, although the chip has not yet reached its original target of 50 MHz. The company is making the chip generally available to customers that want it, but does not plan a full-blown marketing campaign. Motorola has designated a single group to provide sales support for both the 88110 and its PowerPC line, another sign of its ongoing de-emphasis of the 88K line. The 88110 will be relegated mainly to embedded applications, with the exception of the few remaining vendors of 88000-based systems. IBM announced a new X-terminal using the 88110, but admits that the product will probably migrate to the PowerPC 601 once that chip reaches full production.

The 88110 is a flexible superscalar processor with speculative instruction execution and an on-board graphics unit (see µPR 12/4/91, p. 1). Although the company produced first silicon well over a year ago, the chip has been beset by both functional and frequency problems. At this time, the chip is in production at 40 MHz but is still having problems at its original target frequency of 50 MHz. Motorola hopes to ship 50-MHz chips in volume by the end of the first quarter.

The company claims that current parts are fully functional but it has not made any performance measurements available, stating that it will be up to system vendors to announce performance. At the Microprocessor Forum in 1991, Motorola revealed that it had simulated a 50-MHz 88110 at 51 SPECint89 and 74 SPECfp89 with no external cache. Assuming the real chip performs as simulated, actual SPECmark92 numbers are probably both in the 50–60 range. The company did reveal pricing: $360 at 40 MHz and $495 at 50 MHz, in 1000s.

Given these figures, the 40-MHz part should offer about the same performance as a 33-MHz SuperSPARC but at a lower price. The 50-MHz part should offer Pentium-class performance at 486DX2 prices. While this may sound attractive, the performance is far behind the top chips from DEC and HP. Furthermore, the lack of an installed base has left few vendors interested in the 88110 as a general purpose CPU. Only Harris has so far committed to releasing systems based on the chip. Data General, the only significant system vendor using the 88000, has yet to announce its intentions. Despite this apparent lack of interest, Motorola says that it is forging ahead with a follow-on to the 88110.

AMD and HP Cooperate on New IC Process

Hewlett-Packard and Advanced Micro Devices said that they will work together to develop a 0.35-micron CMOS process. The new process, expected to be in volume production in 1995, will allow five to ten million transistors to be placed on a single chip. Contrary to some reports, HP and AMD will not work together on CPU chip design, and no licensing of either the PA-RISC or 29000 architectures is involved. The process development will involve engineers from AMD's Submicron Development Center in Sunnyvale and HP's Deer Creek facility in nearby Palo Alto. Once development is complete, HP plans to use the new technology at its Corvallis, Oregon fab, while AMD will deploy it at Fab 25 in Austin.

The agreement is similar to one signed about a year ago between HP and Analog Devices to codevelop a 0.55-micron CMOS process. Like AMD, Analog participates in markets that are complementary to HP's, so there is no direct competition between the partners. Today, HP and Analog have nearly completed their development work; HP is now sampling 0.55-micron chips and expects to have the new process in production by this summer. HP's PA7100 uses a 0.75-micron (effective) process, the company's current top-of-the-line.

BIT Closes Fab–No More ECL Processors

Bipolar Integrated Technology, the only remaining champion for ECL processors, announced that it will close its manufacturing facility and become a fabless design house. The future of the company is in doubt if it does not quickly find customers for its design services.

The announcement tolls the bell for merchant-market ECL processors. (Some in-house ECL work continues at both DEC and Sun research labs.) BIT led the charge in this direction with the MIPS-architecture R6000 and the B5000 SPARC processor. Both operated at then-impressive frequencies of 66–80 MHz but required expensive multichip designs. The R6000, featured in Control Data's MIPS-based systems, also proved difficult to manufacture. Ultimately, CMOS processors surpassed the speed of ECL chips with much lower costs, leaving BIT as a footnote in microprocessor history.

Micro Channel Speed Clarification

In our 12/30/92 issue *(see **061703.PDF**)*, we stated that the Micro Channel uses a 10-MHz clock. The Micro Channel Developer's Association has asked us to clarify that the Micro Channel specification supports a 20-MHz clock, and prototype systems running at this speed have been demonstrated. Existing Micro Channel PCs and system-logic chip sets, however, are limited to the 10-MHz rate.

Errata: Trident Price Correction

Due to incorrect information from the vendor, we quoted inaccurate prices for graphics accelerator chips from Trident Microsystems in our 12/9/92 issue. The correct price for the Storm DG (TGUI 9420) is $31.50; the correct price for the Storm VG (TGUI 9430) is $48. ♦

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