THE EDITOR'S VIEW

Clouds Darken Over RISC

Some Will Perish After Introduction of Intel/HP Architecture

RISC processors, unless they're home grown, are becoming less and less interesting to system vendors. NEC's rejection of MIPS chips for its systems *(see* **1014MSB.PDF***)* is another sign of the times; the Japanese company is nominally switching to HP's PA-RISC, but the real destination is the future Intel/HP architecture, IA-64. As IA-64 becomes a reality, we expect other vendors to follow NEC's lead. Ultimately, this trend could result in one or more RISC processor vendors giving up on their architectures.

Nearly every major computer company today is either building systems around x86 chips or using its own in-house RISC processor (or both). Apple, of course, gets its processors from IBM and Motorola, but the Mac vendor's involvement in PowerPC is so intimate that it hardly counts as an exception to this rule. Fujitsu is a staunch SPARC system vendor but consumes many processors from its Ross and Hal subsidiaries. Otherwise, the largest computer vendors making significant use of an externally produced RISC processor are Tandem and Pyramid, midsize players at best.

This situation leaves Digital, HP, Silicon Graphics, and Sun with so-called MORPs: my own RISC processor. The volume of chips such as the 21164, PA-8000, or R10000 is truly miniscule, a few tens of thousands per year. Under the old business model, high-end processors like the R4000 would eventually migrate into low-cost systems, pumping up their lifetime volume. In today's competitive market, recycled high-end chips are no longer adequate for the low end; instead, vendors are designing price/performance products like the R5000 and the PA-7300LC, preventing high-end chips from ever reaching volume price points.

If high volumes are never attained, conventional economics says the cost of developing a beast like the R10000's follow-on must be spread across the miniscule volume of parts ultimately produced, resulting in a huge surcharge per chip. The RISC vendors claim the revenue from their systems is more than enough to cover this cost. Each of the MORP vendors collects several billion dollars per year in RISC system revenue. The cost of maintaining a couple of hundred processor designers is perhaps 1% of that revenue.

These vendors are willing to bear this cost because they gain a competitive advantage: better performance, particularly on floating-point applications, than mass-market processors can provide. Furthermore, the costs of moving their user base to a new architecture are daunting, even if that architecture would eliminate the need for internal CPU development. Thus, no vendor has followed HP's lead in terminating its RISC architecture.

That may change in a few years, however. Today's out-of-order RISC processors are overburdened with the very complexity that RISC was intended to eliminate. Too little of the chip is doing real work; the rest is devoted to keeping two sets of books, in case the software ever conducts an audit to find out what the CPU has really been up to. While it is certainly possible to work with a balky architecture (witness the success of x86), the performance growth rate of RISC architectures will be difficult to maintain.

HP, with Intel's help, aims to solve this problem by moving to IA-64, a clean new architecture that we believe will push much of this complexity back into the compiler, boosting performance by devoting more of the chip to instruction execution. Because of this leap forward, we expect Merced, the first IA-64 processor, to outperform all traditional RISC processors. HP will solve the migration problem by offering compatibility with PA-RISC, probably through some sort of translation/emulation scheme.

Other RISC vendors will then be faced with some difficult choices. Staying with current instruction sets will probably put them at a performance disadvantage to IA-64. To close this gap, they could develop a new instruction set along the lines of IA-64, but such a massive development effort, as well as moving customers to that instruction set, will be more expensive than maintaining the existing product line.

Once the thought of a new instruction set is on the table, another option is to simply adopt IA-64. This move eliminates the cost of in-house development while ensuring performance competitiveness. If buying processors from Intel is unthinkable, vendors could instead band together to develop a competitive instruction set, sharing the development costs and building more volume for the new design.

SGI can easily differentiate its products on the basis of 3D performance, regardless of the underlying CPU; the company is a good candidate to switch to IA-64 or Project 2K, a new instruction set under development by the PowerPC vendors *(see* **101103.PDF***)*. It is less clear how Sun or Digital would differentiate their products from those of other IA-64 vendors. Digital seems likely to stick with Alpha until the bitter end, which, given the company's recent return to unprofitability, may be sooner than later. Sun may stay with SPARC or join an anti-Intel alliance. Efforts to rival IA-64, however, are already two years behind; so far, this delay is probably not fatal, but the clock is ticking for these vendors. M