Toshiba, TI Roll Out Set-Top Box Chips

All-in-One Designs Couple Embedded CPU Cores with Substantial Logic

by Jim Turley

Texas Instruments and Toshiba have nearly simultaneously announced single-chip decoders for digital satellite and cable television receivers. Both are based on embedded microprocessor cores and offer simple solutions for DVD, digital satellite system (DSS), and digital video broadcast (DVB) applications.

Toshiba's TC81220F includes an R3900 MIPS core and an enormous amount of special on-chip logic, as Figure 1 shows. (This is the same CPU core General Magic and Philips use in their PDA platforms; see **1017MSB.PDF**). Specialized I/O includes a programmable transport processor, an MPEG-2 audio/video decoder, synchronous DRAM (SDRAM) interface, DMA, smart card reader, video-DAC interface, and IEEE-1394 (FireWire) interface.

To make a complete system, the chip requires little more than 2M of SDRAM for its MPEG decoding workspace, 512K of standard DRAM for system memory, and a PAL, SECAM, or NTSC encoder for the video. Including the memory and analog components, the complete semiconductor budget for a satellite receiver box is only about $100, according to Toshiba.

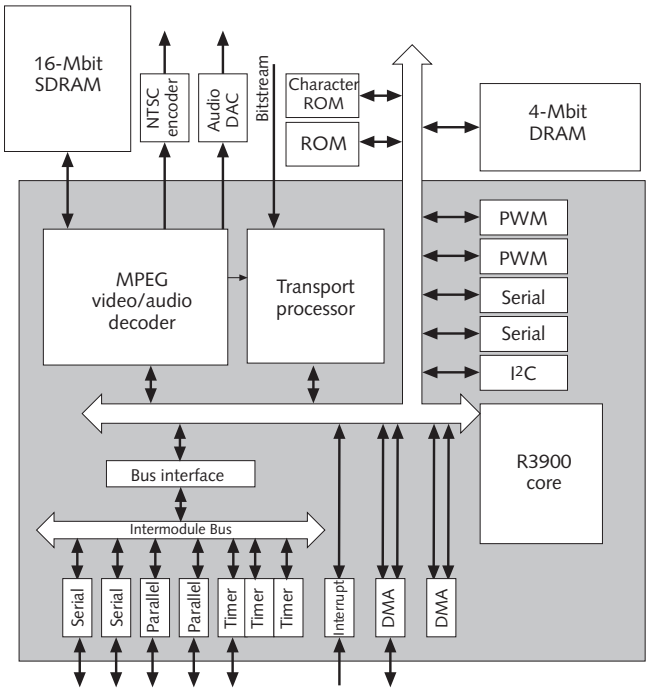

Figure 1. Toshiba's TC81220F satellite television decoder includes several autonomous units, including an R3900 MIPS core and a programmable transport processor. With 512K of DRAM, 2M of synchronous DRAM, and some analog components, the chip can implement a complete DSS system.

Price & Availability

Texas Instruments is sampling the TMS320AV7100 now, production is scheduled for 2Q97; the '7110 will begin sampling in February, with production in 2Q97. In 100,000-unit quantities, both parts are priced at $45. For more information, contact TI (Denver) at 800.477.8924, extension 4500.

Toshiba's TC81220F will begin sampling in 1Q97 in a 208-lead PQFP package; production is scheduled for 3Q97. The part is priced at $45 in 100,000-piece lots. For more information, contact TAEC (San Jose, Calif.) at 800.879.4963.

TI's approach is similar to Toshiba's, integrating everything necessary for a digital receiver into a single chip. The TMS320AV7100 uses a 40-MHz ARM7 core with Thumb (see **090401.PDF**), compared to Toshiba's MIPS core. (TI's part number officially categorizes the '7100 as a DSP, although there's no evidence that the chip contains one.) Like the 81220F, the '7100 includes an MPEG-2 audio and video decoder, transport processor, FireWire interface, and support for 16 Mbits of SDRAM for a decoding buffer.

TI also offers a second version of its chip, the '7110. The transport layer of the '7100 is designed for DSS (satellite) reception, while the '7110 is tuned for DVB (cable) delivery.

The differences between the two vendors' chips are minor, but may be significant. Unlike the Toshiba chip, the two TI parts include their own NTSC/PAL outputs. They also dispense with the separate 256K×16 DRAM, operating entirely from the 16-Mbit SDRAM buffer.

These parts also differ in integer processing power. Toshiba's 50-MHz R3900 core has more horsepower than TI's 40-MHz ARM7. Both companies suggest using the left-over CPU cycles to add sophisticated on-screen user interfaces; with more CPU cycles to burn, Toshiba's chip presumably can deliver more spectacular on-screen graphics.

With satellite receiver sales booming beyond initial expectations, the time is right for these companies to offer simple, high-volume hardware configurations. Like cellular telephones in the U.S., satellite dishes and decoders are often sold for less than cost or given away with a service contract. Thus, it's crucial these boxes be simple, reliable, and inexpensive to manufacture. These devices should improve the satellite TV delivery mechanism, if not the content. M