At A Glance

SPARC V9 Adds Wealth of New Features 1
The latest version of SPARC, dubbed V9, adds much more than 64-bit address and data capabilities. It includes conditional moves, static branch prediction, and data prefetching, making it comparable to rich architectures such as POWER and Alpha. Several improvements to V8 will improve overall performance.

Editorial: Announcing the MicroSystems Group 3
Mike Feibus has joined MicroDesign Resources to help provide more coverage of system issues such as graphics, buses, and storage. He is organizing this spring's MicroSystems Forum.

Most Significant Bits 4
Intel delays Pentium "announcement"; R4400 delivers impressive benchmarks; IBM provides first details of RIOS 2; Motorola (finally) announces the 88110; AMD and HP cooperate on new IC process; BIT closes fab—No more ECL processors; Micro Channel speed clarification; Errata: Trident price correction.

SGI Provides Overview of TFP CPU 12
Silicon Graphics provided the first details on its forthcoming high-end CPU, code-named TFP. The new MIPS processor combines two chips in a four-way superscalar design with two complete FPUs.

TI Previews High-Performance Video Engine 14
Texas Instruments has described its next-generation video chip, which combines several processors onto a single chip to provide enough power for two-way video conferencing and other activities.

Readers Pick AMD as Top Processor Vendor 15
A survey of our subscribers who design systems showed that they preferred AMD over twenty other chip vendors. Intel, while widely used, received mediocre ratings in several categories.

New DRAMs Improve Bandwidth (Part 1) 18
In the first of a three-part series, we look at alternative DRAM designs. Although Ramtron's enhanced DRAM and the JEDEC synchronous DRAM provide useful extensions to the current design, Mitsubishi's cached DRAM appears to have the most potential.

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MICROPROCESSOR REPORT
THE INSIDERS' GUIDE TO MICROPROCESSOR HARDWARE

Published By
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874 Gravenstein Hwy. So., Suite 14
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Microprocessor Report is published every three weeks, 17 issues per year. Rates are:

N. America: $445 per year, $795 for two years.

Europe: £345 per year, £595 for two years.

Elsewhere: $575 per year, $995 for two years. Additional copies in the same envelope $145 per year in North America, $195 elsewhere. Back issues are available.