

# Smarter Consumer Electronics in Offing

## *International Conference on Consumer Electronics Sees Debut of New Chips*

by Peter N. Glaskowsky

The recent International Conference on Consumer Electronics (ICCE), sponsored by the Consumer Electronics Society of the IEEE, featured a number of interesting presentations describing new chips that will enable a new generation of consumer-electronics products with tremendous processing power, high levels of integration or improved connectivity—or combinations of these features.

Not all of these announcements will turn into commercial devices, but they provide insight into the current state of the art in consumer-electronics technology.

### DTV Chips Multiply

Early chip sets for digital television, which tended to be complex and expensive, are giving way to new chips and chip sets that feature higher levels of integration and lower cost. Several ICCE presentations featured new chips for DTV applications that promise to slash the price of high-definition television (HDTV) receivers from their current \$1,000 and up price levels to mainstream market prices of less than \$500.

A paper from Mitsubishi and Bell Labs described a chip that combines core-logic features with MPEG-2 decoding and a 2D-graphics engine. The chip works with an undisclosed external microcontroller and needs just 6 MBytes of commodity SDRAM for standard-definition applications or 12 MBytes for HDTV. The chip's transport-stream interface supports rates up to 135 Mbits/s, well above the level needed for HDTV, and the integrated up/down conversion block can translate from any supported video resolution into any other. The chip will be implemented in 0.25-micron technology, and it will be offered in versions for standard-definition and high-definition TV.

A presentation from LG described a chip with similar goals, but LG says its product uses a novel compression algorithm and can decode HDTV signals in as little as 4M of DRAM—far less than the 96M required by a brute-force implementation. LG's MPEG-2 decoder also employs aggressive power-reduction techniques. Each calculation unit detects when its coefficients are zero and disables the clock signal for that calculation. LG says it has manufactured this 760,000 gate chip in a 0.35-micron four-layer-metal technology, achieving a die size of 90 mm<sup>2</sup> and a power consumption under 1.5 W at 3.3 V.

Toshiba described a chip for standard-definition applications that includes an R3900 microprocessor core along with a transport-stream decoder, video and audio decoders, a 2D-graphics unit, and a memory controller. The decoders and the graphics unit are all implemented using program-

mable RISC cores. Toshiba says this flexible architecture creates a part well suited to the emerging data-broadcasting applications being built on top of digital TV.

### Picture Processors Boost Display Quality

Siemens offered a look at a chip that provides picture-quality enhancements for standard-definition video. The chip takes in two digital video streams and can perform a wide range of picture processing tasks on these streams, producing a single output stream for the display. These tasks include scan-rate conversion (for example, converting PAL content to NTSC), high-quality picture-in-picture presentation, and split-screen video, even for sources with independent timing. The chip's scan-rate conversion engine uses an MPEG-like motion-detection algorithm that produces high-quality intermediate frames and eliminates most sources of motion jitter. A unique feature of the chip is the incorporation of twenty-four 256-Kbit embedded DRAM cores as a frame buffer.

IBM and Snell & Wilcox presented a picture processor of their own, a chip designed primarily for up-conversion. The chip converts interlaced, low-frame-rate standard-definition content (like NTSC broadcast video) to progressive-scan, high-resolution, high-frame-rate video. Chips such as this will be used in future HDTV sets to make SD content look more like HD. This chip has been manufactured using 0.5-micron three-layer-metal technology with a die size of 56 mm<sup>2</sup> in a 208-pin package.

Philips offered two presentations related to a chip set for TV control and picture-quality enhancement. The set includes a 48-MHz MIPS R3000-class processor that supports the MIPS II and MIPS-16 instruction sets. The processor chip also includes at least 10 peripheral subsystems interconnected by a PI-bus. These include a 2D-graphics engine, an SDRAM controller, and a soft-modem line interface. This TV telecommunications and control processor (TCP) is a commercial product, available now. The TCP is manufactured in a 0.35-micron CMOS process with five metal layers; it has a die size of 80 mm<sup>2</sup> and comes in a 352-contact BGA package.

The other half of the Philips chip set is a PI-Bus coprocessor for picture enhancement. It handles even more functions than the Siemens chip, adding adaptive temporal noise reduction (a feature that identifies and removes noise that changes from one frame to the next), sharpness enhancement, and a color-space converter. Philips is aiming this chip set at intelligent televisions, especially those running the Windows CE operating system, which the chip set is specifically designed to support.

### “Soft” DTV Evaluated

The Tampere (Finland) University of Technology presented its analysis of host-based HDTV decoding using Sun's Ultra-Sparc processor. The group's software uses Sun's VIS instruction-set extensions. On a 360-MHz processor, the software decoder could keep up with standard-definition PAL content (25 frames per second (fps) at  $720 \times 576$  pixels) at a source data rate of 5–7 Mb/s.

HDTV content, which requires almost five times the processing resources, is decoded at about six frames per second. The group also tested a dual-processor 360-MHz Ultra-Sparc system, which achieved 11 fps. Based on these results, we expect to see mainstream microprocessors capable of pure software decoding of HDTV content within a few years. It is likely to take another year for this capability to arrive on real-world desktop PCs, since robust HDTV decoding requires substantial performance headroom to handle other tasks, such as the user-interface management.

### MPEG and JPEG Codecs Get Cheaper, Faster

Two presentations described single-chip MPEG-2 codecs that can handle video encoding and decoding. These parts will compete directly with chips from C-Cube (see MPR 12/8/97, p. 1) and other vendors in consumer-electronics products like digital camcorders and video-editing systems.

Sanyo's chip is designed to support half-resolution NTSC video ( $360 \times 480$  pixels) for low-bit-rate camcorder applications. Sanyo says that even at just 3–4 Mb/s (one-eighth the rate of today's digital camcorders), this chip achieves “satisfactory” visual quality. Sanyo says the chip consumes just 0.5 W and is less than  $87 \text{ mm}^2$  in size in a 0.25-micron four-layer-metal process. The chip includes 710,000 gates plus 140 Kbits of SRAM.

A chip developed by Hitachi supports full-resolution video at data rates up to 6 Mb/s, as well as a still-picture mode with a resolution of  $1,280 \times 960$  pixels. Hitachi says its chip will be manufactured in a 0.18-micron process.

Sanyo also described a chip designed specifically for still cameras. In this application, MPEG is not needed; Sanyo's chip uses JPEG compression, like most digital cameras. The Sanyo device is meant to provide all the necessary logic for a digital camera except for the CCD and memory; it includes a 28.8-MHz RISC processor, a CCD signal processor, a JPEG compression engine, a memory controller, and an LCD interface. Sanyo's JPEG engine is capable of compressing VGA-resolution images at 47 frames per second, which suggests it could compress  $1,600 \times 1,200$ -pixel images at about 7 fps—much faster than today's cameras. Sanyo says the chip has been manufactured in a 0.35-micron three-layer-metal process and is about  $110 \text{ mm}^2$  in size. Power consumption was measured at 700 mW maximum.

### IEEE 1394 Extends Reach

Although the IEEE 1394 standard is the subject of great debate in the PC market, 1394 is already well entrenched

### For More Information

The *Digest of Technical Papers* from the 1999 International Conference on Consumer Electronics is available for \$146 from the IEEE Operations Center (#99CH36277). The center may be reached at 800.678.4333. More information on ICCE is available online at [www.icce.org](http://www.icce.org).

among consumer-electronics makers. As it exists today, 1394 has certain limitations that inhibit wider use. These include a lack of electrical isolation between endpoints as well as a maximum wire length of just 4.5 meters, not adequate to connect 1394 devices throughout a house or even a large room. There are proposals to address these limitations, including an optical implementation that uses plastic optical fiber. NEC's Media Research Labs presented two new proposals that go even further to expand the reach of 1394.

The first of these presentations involved a wireless 1394 translator based on infrared LEDs and photodiodes. The design achieves a range of 10 meters while allowing up to five degrees of misalignment, which NEC believes is sufficient for room-area applications. NEC's current experimental translator operates at 200 Mb/s, enough for most 1394-equipped products; the company is working on a faster version. NEC says that one of its concerns was ensuring an eye-safe design, since the device emits about 20 mW of infrared energy at 850 nm. This was achieved by a lens system that effectively increases the size of the emitting area, preventing any risk to the user.

NEC's other 1394 presentation described a long-haul translator that extends the reach of a single 1394 link up to 500 meters over unshielded twisted-pair wire or a glass optical fiber. The translator combines 1394's separate clock and data signals, using a new coding scheme to eliminate signal skew. This scheme is consistent with the forthcoming 1394 standard for faster speeds (800 Mb/s and up). Like NEC's IR adapter, this experimental device also operates at 200 Mb/s.

### Consumer Electronics Borrows From PC Market

Much of the technology used in these devices was first tested and proved in the PC market. JPEG was developed to compress images on PCs; MPEG was meant to bring the benefits of compression to video products, but it also found its first widespread success in PCs. Similarly, much of the progress in video enhancement has been made by PC graphics vendors. 1394 technology came from Apple, which hoped to use it as a peripheral connection on Macintosh computers.

All of these elements are leading to a new generation of consumer-electronics products that have far more computing power and better communication abilities than the PCs of just five years ago. Perhaps television programs won't get any better, but the television set itself certainly will.  $\square$