Cyrix Creates Ultimate CPU for Games

New Integrated Processor Combines Cayenne's Core, Hardware 3D Engine

by Peter N. Glaskowsky

Not content to let its new Cayenne core get all the attention at October's Microprocessor Forum (see MPR 10/27/97, p. 22), Cyrix also disclosed a highly integrated Cayenne derivative called the MXi. The new chip, described by MXi project manager Doug Beard, is the latest in a series of Cyrix processors with integrated memory and graphics controllers and will mark the first appearance of the Cayenne core.

Like the first chip in the series, the MediaGX, the MXi drops Socket 7 compatibility in order to include various on-chip peripherals. Cyrix has equipped the new chip with the widest, fastest main-memory interface found on any x86 processor, a full-featured 2D/3D graphics accelerator with a fast virtual AGP bus, and hardware DVD playback logic, as Figure 1 shows.

Implementing all these features will require nine million transistors, but Cyrix estimates the MXi's die size at just 90 mm^2 in a 0.25-micron process with five metal layers, allowing the new chip to be priced at or below the combined cost of any comparable x86 CPU with a separate 3D graphics chip. If the chip reaches its aggressive performance targets, however, Cyrix may charge a premium price.

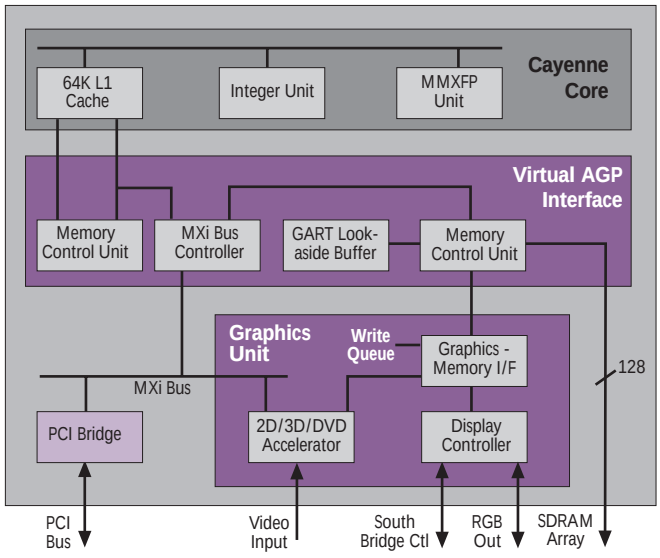

Figure 1. The Cyrix MXi includes the general-purpose Cayenne core for x86 compatibility and enhanced 3D-geometry performance, an AGP-compliant memory controller and graphics interface, and an integrated 2D/3D/DVD graphics subsystem that should match or beat the performance of discrete solutions.

MXi Has Fast Memory, But No Cache

Apart from the advantages of having a 3D accelerator integrated onto the die, Cyrix's decision to provide a high-performance SDRAM memory interface on the MXi should provide a big performance boost for applications that don't benefit from L2 caches—but conversely, the omission of an L2 cache means that common desktop applications are likely to suffer.

Like Cayenne, the MXi has a 64K unified L1 cache, but few applications have critical code segments that will fit entirely into such a cache. With an integrated memory controller, the MXi's memory-access latency will be significantly lower than that of other processors, but still at least 20 ns for page hits and 60 ns for more-common page misses, vs. 15 ns for a typical L2 cache.

The MXi's memory interface supports pipelined memory transactions to a 128-bit SDRAM array at clock rates of at least 133 MHz, yielding more than 2 Gbytes/s of peak bandwidth. The MXi is also compatible with the forthcoming double data rate (DDR) SDRAM, which could further increase the effective throughput of the memory subsystem. For applications that don't benefit from L2 caches, the MXi's memory architecture should produce very impressive performance. Cyrix hasn't suggested using the MXi in database engines or Web servers, but it should perform well on such tasks.

The primary markets for the MXi—3D gaming and multimedia—are also typified by data sets that greatly exceed the size of L2 caches found on today's PCs. The vertex data and texture maps found in 3D scenes can reach several megabytes in size, and many multimedia functions, like MPEG-2 playback and high-quality MIDI sound synthesis, also require large data sets. These applications should perform very well on the MXi, especially given the Cayenne core's inherent performance. Cyrix has not announced specific speed grades for the MXi, but the company expects to offer chips roughly as fast as a 300- to 400-MHz Pentium II processor on typical desktop applications. Our analysis suggests that software DVD decoding with two-channel Dolby Digital audio should require no more than 60% of the fastest MXi processor.

Integrated 3D Distinguishes the MXi

The most interesting thing about the MXi is its integrated 3D-graphics engine. The graphics controller, which also provides 2D and MPEG-2 acceleration features, shares the main memory with the CPU in a unified memory architecture (UMA). This UMA design is less like previous PC-based UMA efforts with conventional memory subsystems

(see MPR 6/19/95, p. 1) and more like that of Silicon Graphics' O2 workstation, which also uses an unusually fast main-memory array to achieve high graphics performance.

Cyrix has not released internal details of the 3D core, but the company's performance estimates suggest the chip will rank among the fastest 3D chips available next year. The bilinear-filtered texture fill rate is estimated at 120 Mpixels/s, which translates to a texture-read bandwidth of 960 Mbytes/s. Since the MXi's main memory can provide this much bandwidth directly, a texture cache is almost unnecessary, but Cyrix has included 4K of texture cache anyway. This is smaller than the texture caches found on today's best 3D chips, but it should satisfy enough texture fetches to justify its minor impact on die size and complexity.

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Cyrix project manager Doug Beard describes the MXi's integrated 3D accelerator.

The MXi's polygon throughput is rated at 2 Mtriangles/s, which should exceed that of most discrete mainstream 3D chips in 2H98. This level of performance is achieved by a combination of accelerated geometry processing in the core and a fixed-function setup accelerator in the 3D engine. The MXi should be able to provide real-time performance—frame rates of 60 Hz or more—on 3D scenes with roughly 20,000 visible triangles, or about four times the scene complexity found in current 3D software. With AMD and Centaur (but not Intel) also planning 1998 shipments of processors with similar 3D geometry performance (see MPR 12/8/97, p. 4), the MXi's advantage (if any) will come from the closer ties between its 3D hardware and main memory, which will speed the transfer of triangles from applications to the screen, and presumably a lower system cost.

AMD, Centaur, and Cyrix plan to use the AMD 3D extensions in accelerated host-based geometry code for Microsoft's DirectX 6.0, due out early next year. In contrast to the original plan, which would have required ISVs to use proprietary Cyrix extensions, the new scheme will allow ISVs to benefit from the AMD 3D extensions just by using Direct3D's software geometry engine. For applications that don't take advantage of the new 3D extensions, transform and lighting calculations are performed in the Cayenne core's x86 FPU, which we estimate will be able to process only about 1.2 Mtriangles/s, or roughly 60% of the peak throughput of the MXi when the AMD 3D extensions are used. Even so, the MXi's integrated architecture should permit better overall performance than mainstream Pentium II systems can achieve.

Since most desktop applications—including the Windows graphical user interface itself—use only 2D operations, 2D performance is still critical in the PC market. In general, GUI acceleration is a function of bandwidth between the CPU and the 2D chip, and between the 2D chip and the frame buffer; here, the MXi's closely coupled design is ideal. Cyrix claims a 1.6-Gpixel/s fill rate and 800-Mpixel/s block transfers (BLTs) for 8-bit pixels, comparable to the performance of today's best 128-bit graphics chips.

The MXi's graphics engine also accelerates the final stages of DVD decoding. Cyrix licensed the necessary logic for MPEG-2 motion compensation from Mediamatics and also includes color-space conversion, scaling, filtering, and DVD subpicture blending functions in its chip. These features, common in many of today's mainstream 3D chips, reduce the amount of processing the CPU must perform during DVD playback.

Figure 2 shows the essential components of an MXi-based system. Since the MXi comes with a Cyrix-designed "south bridge" chip with internal RAMDAC and ISA bridge, OEMs need to add only SDRAM and the appropriate peripheral chips to form a complete system.

Virtual AGP Ensures Compatibility

The graphics subsystem is connected to the CPU and main memory via a virtual AGP interface. Although these on-chip connections are not physically compatible with AGP, and there is no external AGP interface, the MXi provides a full set of AGP-compatible control registers as well as the graphics address remapping table (GART) required by the AGP specification. Cyrix will provide the necessary AGP software driver to OEMs that purchase the MXi, making the chip fully compatible with all AGP-aware 3D software.

Beard claims this virtual AGP interface is effectively faster than the 4×-mode AGP interface that Intel plans to design into chip sets in late 1998, but this is not completely true. Even today's Pentium II systems with 2×-mode AGP have more net bandwidth than the MXi for certain operations. If such a system is equipped with a 128-bit 3D chip such

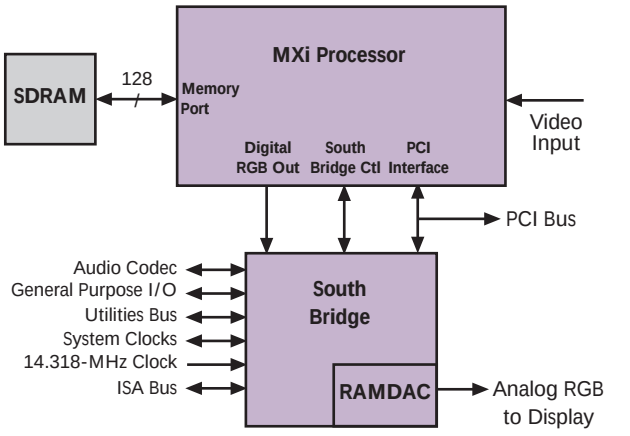

Figure 2. The MXi processor comes with its own "south bridge" chip that includes a RAMDAC and ISA bridge. OEMs can produce complete systems by adding a few commodity peripheral chips.

Price & Availability

The MXi processor is expected to ship in 2H98; Cyrix has not disclosed pricing. For more information on the MXi and other Cyrix processors, access the Web at *www.cyrix.com/process/prodinfo/prodin-p.htm*.

as Nvidia's RIVA 128, it has approximately 1.2 Gbytes/s of peak bandwidth between the CPU and the L2 cache, plus 533 Mbytes/s between main memory and the CPU and/or 3D chip, plus 1.6 Gbytes/s between the 3D chip and graphics memory. The MXi shares its 2-Gbyte/s main-memory array between the CPU and graphics, and it has no L2 cache or separate graphics memory.

Thus, applications that fit into a 512K L2 cache and do texture mapping from local graphics memory will see better overall performance even on these 1997 Pentium II systems. By 2H98, the MXi will be at a greater disadvantage in this specific situation as processors, AGP, and 3D chips all get faster.

MXi Could Dominate Low-End PC Market

In its target market of low-cost PCs, however, Cyrix should be able to make an unbeatable price/performance argument for the MXi. Without a separate PCI host bridge ("north bridge"), graphics controller, or graphics memory—components that typically add $50 and several square inches of board space to the cost of a motherboard—the MXi can be priced below the equivalent functions from competing vendors while offering the same, or better, overall performance. Systems equipped with the MXi and selling for less than $1,200 should provide all the 3D and multimedia performance of most midrange $2,000 machines.

The MXi may find a role in even lower-priced systems that could be sold as Windows-compatible video games to compete at the high end of the game market currently dominated by Sony's Playstation and the Nintendo 64. Indeed, if Cyrix chooses to sell the MXi for around $100, it could be used as a 3D accelerator on high-end graphics cards. The MXi should match the performance of high-end 3D chips in 2H98, especially on OpenGL applications that can use the MXi in this configuration as a geometry accelerator.

If the MXi meets its goals of 400-MHz Pentium II CPU performance and leading-edge 3D performance, Cyrix may initially choose to charge a premium price, leaving the GXm version of the MediaGX to carry on in low-cost PCs. Ultimately, however, the MXi should drop down into low-end systems like the MediaGX-based Compaq Presario 2200, providing strong performance at a minimum price. M