XSIM: AN EFFICIENT SIMULATOR FOR CROSSTALK ANALYSIS BETWEEN ON-CHIP INTERCONNECTS

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Abstract

The paper presents an efficient simulator "XSIM" for analysis and modeling of crosstalk between two parallel interconnects in DSM chip. The tool is fast, flexible, easy-to-use, and yet very accurate.

1. Introduction

In the deep sub-micron (DSM) era, the need for an efficient tool for crosstalk fault analysis in parallel interconnects is well understood by the current SoC designers. This is because the interconnect parasitics and coupling parameters due to the large aspect ratios have become significant [1] in system performance as they can lead to various problems such as, crosstalk delay, speedup and logic hazards. So the accurate computation of glitch voltage and delay variation in the victim due to aggressor is significant in the process of circuit design. With the above objective in mind *Li. et al* has developed the XtalkDelay [2], a crosstalk aware timing analysis tool for chip-level designs. Such tool employs a path-based approach; uses detailed and accurate distributed RC parasitics for critical nets and their aggressors; uses BSIM3-accurate gate models and invokes finally HSPICE for delay computation using only the minimum required set of input patterns. Similarly, here we propose an efficient tool "XSIM" for analyzing and modeling the crosstalk faults, both in defective and defect-free interconnects, and its methodology using the distributed ABCD model.

XSIM takes into account the distributed RLGC parasitics of interconnect, distributed coupling capacitance and mutual conductance between interconnects, length of interconnects and also the RC linear models of the CMOS drivers and receivers of both aggressor and victim. The tool is easy-to-use because of user-friendly implementation of GUI in C++, and flexible because of the possibility of selecting any combination of input signals including the *skewed ones* to compute various crosstalk coupling effects between interconnects. The remaining part of the paper is organized as follows: Section 2 describes the brief methodology followed by experimental simulations carried out with XSIM tool in Section 3. Finally, Section 4 concludes with brief remarks.

2. Methodology of XSIM

The XSIM tool is developed based on the distributed ABCD models of the parallel interconnects' pair. The reason for using such distributed model is that the model becomes very accurate because of the consideration of distributed RLGC parasitics, *i.e.* resistance, inductance, conductance and capacitance *etc.*, and also distributed mutual capacitance and mutual conductance between the interconnects.

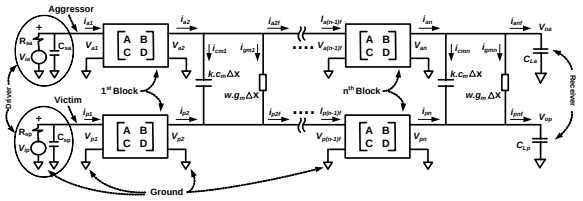

Figure 1: Distributed ABCD model of two parallel nets

Figure 1 shows the distributed ABCD model of a pair of parallel interconnects including the RC modeling of CMOS drivers, and capacitive loads of CMOS receivers. Here, each ABCD block of interconenct length Δx contains interconnect's RLGC parasitics. In Figure 1, the coefficients k and w of the coupling capacitance and mutual conductance respectively characterize the defect [4] due to bad etching/manufacturing. Now, adopting the similar procedure as shown in [3] the victim's output from such a model can be written as:

$$V_{op}(s) = \frac{2T_1(s)}{(T_1T_4 - T_2T_3)} \cdot V_{ia}(s) + \frac{2T_2(s)}{(T_1T_4 - T_2T_3)} \cdot V_{ip}(s), \quad (1)$$

whereas, the corresponding aggressor output is:

$$V_{oa}(s) = \frac{-2T_3(s)}{(T_1T_4 - T_2T_3)} \cdot V_{ia}(s) + \frac{-2T_4(s)}{(T_1T_4 - T_2T_3)} \cdot V_{ip}(s). \quad (2)$$

The terms $V_{ip}(s)$ and $V_{op}(s)$ in (1) and the terms $V_{ia}(s)$ and $V_{oa}(s)$ in (2) represent the input and output signals of the victim and aggressor respectively in s (Laplace) domain. The fourth order approximation of $T_j(s)$ term from the numerators is:

$$T_j(s) = t_{j0} + t_{j1}s + t_{j2}s^2 + t_{j3}s^3 + t_{j4}s^4; \quad j = 1, 2, 3, 4.$$

Obviously, terms t_{j0} through t_{j4} are functions of interconnect parasitics including the terms mutual capacitance and mutual conductance and linear parameters of drivers and receivers' models. Each term from t_{j0} through t_{j4} is obtained by summing one or more convergent infinite series.

The flow chart of the algorithm used for the XSIM tool is described in Figure 2. Initially, the algorithm calculates the coefficients (terms t_{j0} through t_{j4}) with the parameters of interconnects, drivers and receivers. Now, depending on the input signals combination, the algorithm substitutes the appropriate signals in *s*-domain for aggressor and victim inputs in (1) and (2). Thereafter, by finding the partial coefficients, the algorithm applies partial fraction method on (1) and (2), followed by inverse Laplace transformation to find the time domain representation of output signal waveforms of victim and aggressor respectively (See [3] for detailed procedure). The time domain representations are very important as they provide much useful information about the transmission signal quality (integrity) over long interconnects. Finally, the algorithm simulates and provides the output waveforms within the user required time span. Furthermore, applying the Newtons-Raphson's numerical method on the victim's time domain output waveform, the algorithm determines the victim's 50% delay time or the time of occurrence of crosstalk maximum glitch and glitch height [3]. If the estimated delay time or the crosstalk glitch height is found to be greater than that of it's permissible limit, then the selected value of the influencing parameter is considered to cause signal integrity loss. This, in effect, helps in determining the critical values of the influential parameters, below which the device will continue to behave as fault tolerant.

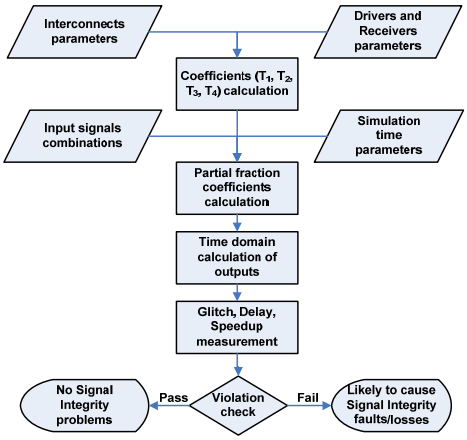

Figure 2: Flow chart of XSIM

3. Experimental Simulations

Here, we describe a few simulation results carried out using the XSIM tool for analysis of crosstalk faults. Figure 3 depicts the simulation results when aggressor has rising input transition and victim has static zero signal. In this case crosstalk glitch is produced on the victim's output signal due to the coupling between interconnects. Logic faults will occur if the glitch amplitude and duration are large enough over the upper-threshold of logic low. Similarly, several simulations were performed to demonstrate the delay violations and reliability problems caused due to crosstalk. It has been observed that the tool is at least 11 times faster than the commercial simulator like PSPICE, whereas it is as accurate as latter. The results obtained were found to be in good agreement with PSPICE, but not depicted here due to space restrictions.

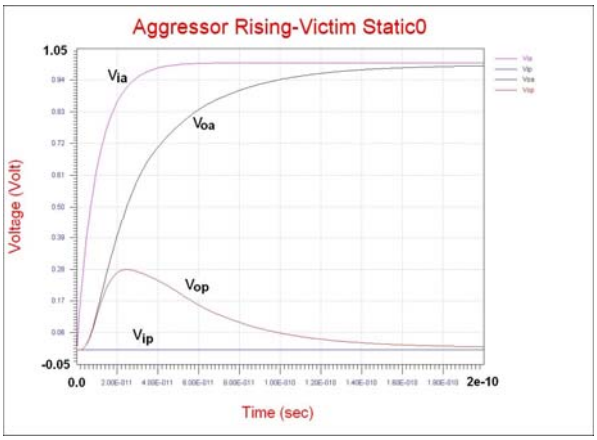

Figure 3: Crosstalk glitch on Victim

4. Conclusion

In this project, we have developed a new crosstalk simulator tool namely, "XSIM" for analysis of various crosstalk faults, such as delay timing violation, logic hazards *etc*., caused due to coupling capacitance and mutual conductance (if any). The tool is based on the distributed ABCD model of parallel interconnects, mutual capacitance, mutual conductance, length of interconnects, and linear RC models of drivers and receivers of both aggressor and victim. The tool has a user-friendly GUI which makes the tool not only very easy-to-use but also flexible. It has been observed that the tool is as accurate as commercial simulator like PSPICE and at least 11 times faster than the latter. Consideration of mutual inductance into the tool is currently left as the future perspective of this work. Apart from the above, the crosstalk simulation of multi aggressor-single victim feature needs to be also incorporated into our future version of XSIM tool, although the same feature is readily available in MATLAB source code.

5. References

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[3] A. K. Palit, K. K. Duganapalli, W. Anheier, "A New, Flexible and Very Accurate Crosstalk Fault Model to Analyze the Effects of Coupling Noise between the Interconnects on Signal Integrity Losses in Deep Submicron Chips", *IEEE-ATS* 2005, December 18-21, Calcutta, India, pp. 22 - 26.

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