

# CAD tools dedicated to the design and test of RFICs

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## Abstract

*A set of small but efficient software tools are presented, which aid the RF designer in his difficult task of establishing an optimized circuit topology and to test the experimental prototype.*

## 1. Introduction

The design of RFICs is becoming more and more complex with the increase of the frequency of interest and when the overall system integration is a matter of concern. While modern CAD frameworks offer impressive performances, so far finding the good circuit topology for a given building block is still under the responsibility of the designer, and the latter also has to decide of the first set of parameter values, with these values as close as possible to optimal ones – even if fine tuning will be done thanks to the CAD framework at the end. To help the designer finding a good set of starting values, specialized and easy-to-use software tools are welcome.

Not only the design of RFICs is complex today : the test of these ICs is even more difficult, as due to the increased integration level access to critical nodes within the circuit is, for the most, a severe challenge – if not an impossible one. Among the test techniques the use of a LASER beam is a potential solution to this problem of node access. Indeed, being contact less the beam can initiate electron-hole pairs almost everywhere at the surface of a given die, and thus active current can be generated which can be brought into play for testing and validation of a circuit. Meanwhile, physical mechanisms appearing within the silicon when the LASER beam is applied are themselves dramatically complex, and the analysis of the circuit response to the beam is not at all obvious. Here again, highly specialized software tools are of great help for the designer to be able to understand his circuit behavior and to validate its topology or its robustness in severe environments.

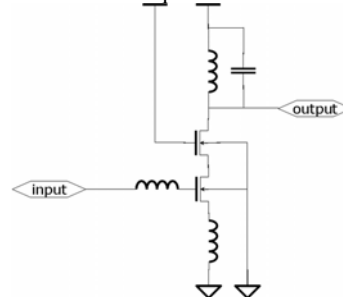
In this paper several dedicated software tools such as the ones before mentioned are presented, the combination of all being of great help for the designers of RF integrated circuits and systems.

## 2. Low Noise Amplifier design tools

While many topologies are available when one consider designing a RF Low Noise Amplifier (LNA), the by far

most encountered circuit is, today, the tuned cascode implementation as depicted in Fig. 1 in its CMOS version.

To summarize, in this architecture the source degeneration inductor is used to balance the Gate-to-Source capacitor of the input transistor at the frequency of interest and, combined with the inductor added in series with the gate the impedance seen at the input of the circuit is made real. Thanks to this approach, the input matching can be optimized for both noise and power transmission.



**Figure 1:** CMOS cascode LNA

The calculation of passive component values is not that much complicated, though expressions are somewhat awkward so a little software able to automatically compute the values, based on the center frequency of interest and parasitic passives associated with a given technology, is very useful.

Also, a software tool able to calculate the inductor values based on the inductor shape is valuable for a designer. Based on basic equations, valid for only a given frequency range and a selected set of generic shapes, this tool can rapidly calculate an inductor value, assuming that key technology parameters are known. Of course a complex EM tool is then necessary to fine-tune the inductor electrical model, which is mandatory for accurate design, but as such an EM tool is a severe time-consumer starting with the values given by the fast and highly specific tool makes the task easier.

The fact that the LNA input impedance software tool and the inductor computation one require technology parameters as an input make these tools suitable for future design as well as current ones, and the combination of both is a valuable aid for RF designers.

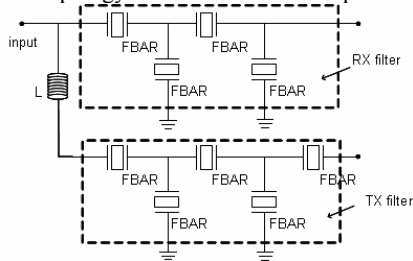
## 3. BAW filter design tool

In transceivers, RF filtering is a key purpose as it allows band selection, emitter versus receiver isolation, and many other critical functions. Nowadays, Bulk Acoustic Wave (BAW) resonators are becoming more and more popular, as

this device can be used either above-IC for System-on-Chip (SoC) implementations or stand-alone for System-in-Package (SiP) ones, increasing the overall system integration level.

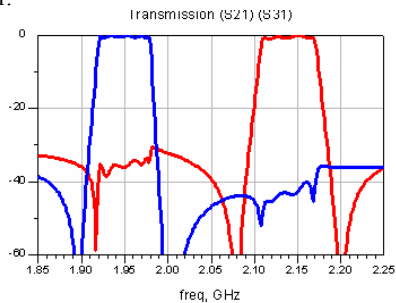
On the other hand, as the filter response relies on the resonator geometries, optimizing the BAW devices is somewhat cumbersome as a lot of parameters have to be considered collectively, and some are correlated with others making the design even more complex.

A dedicated software tool can be used, which requires figures from the considered technology and the filter profile as inputs, and a fitting optimization algorithm yields the final BAW topology suited to the initial requirement.



**Figure 2:** WCDMA duplexer topology

This tool was used to design the duplexer depicted in Fig. 2, with the resulting response of Fig. 3 for a WCDMA transceiver.



**Figure 3:** WCDMA duplexer response.

### 3. LASER testing tools

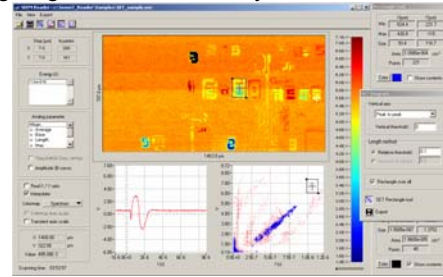
The ATLAS facility of the University of Bordeaux is an experimental platform dedicated to LASER testing and analysis of integrated circuits. The primary applications of this facility are defect localization for failure analysis, fault injection in secured systems, and SEE testing.

A beam line for wavelengths around  $1.3\mu\text{m}$  has been developed for experiments based on the two-photon absorption (TPA) [3]. Adding to the classical 2D resolution of the laser testing technique, the TPA technique is known for providing some kind of resolution in the direction of propagation of the optical beam [4].

Software called SEEM Reader has been developed for analyzing SEE data generated at the ATLAS facility. It is particularly interesting for detailed analysis of Single Event Transient (SET) waveforms. In order to facilitate data exchange, it used an open file format for storing SEU or SET data. It is well suited for - but not limited to - data generated by scanning techniques like laser or micro-beam testing.

Figure 4 depicts the interface of the software with which one can visualize both the signal versus time and the

cartography of the device under test with a color scale highlighting the circuit sensitivity.



**Figure 4:** SEEM tool interface

In Fig. 5 is shown a typical SET cartography of a linear circuit, superimposed on the chip microphotograph. The color scale easily helps the designer to identify critical areas, thus helping in hardening the circuit modifying the layout whenever the sensitivity is considered inadequate.



**Figure 5:** typical SET cartography

### 4. Conclusion

A set of software tools highly specialized have been presented. These tools can be used in association with hugely complex commercial tools such as EM field solvers and circuit simulators, in order to ease the task of designers for either circuit implementations or chip test, being more flexible and low time-consuming.

### 5. References

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