# Specification Validation of Multistandard Transceivers

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## Abstract

*In this demo, we present a design methodology based on a multi-simulator approach instead of using co-simulation, which is dedicated to design complex SoC, including RF and mixed signal.*

## 1. Introduction

The advances in deep sub-micronic technologies will encourage the development of a broader variety of mobile and autonomous communicating systems and devices. In the future, the amount of the exchanged informations between devices will continue to increase. The aim of this project is to develop a methodology and an environment to design future confident objects, able to be interfaced with various terminals and networks. These objects (Fig. 1) will include on the same SoC various communication protocols composed of the different parts: antenna, RF, analog, digital and hardware/software architectures connected with the applicative layer.

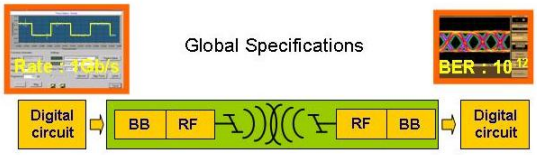


**Figure 1:** Communication system

The (self-) adaptivity of such systems able to operate in various environments (protocols) implies to approach their design in a global way. In order to address the problem of their rapid and global design, we consider analog/digital co-simulation platforms on which it will be possible to model and to verify systems of large complexity. This goal requires to study and to integrate various design flows of circuits and systems in a same simulation framework (SystemC) but also to develop a library of IP-AMS models suitable for the design of these communicating objects.

## 2. Methodology

The different parts (processor, RF, antenna, screen, sensors ...) of complex embedded systems are usually specified and designed separately by engineers working with different EDA tools. In the frame of small communicating objects, it is important to account for critical design parameters (consumption, cost, channel effects) at the system design level in order to early determine the critical parts of the design. It is then important to accurately model the sensitive blocs. During the system architecture preliminary study, one has to be provided a complete hierarchical IP-AMS model library and a unique environment supporting the use of several design flow. In the same way, the test vectors, initially applied at the system level can be reused at each design level.

The simulation time is a very important factor and can be critical. To overcome this limitation, we have introduced four-level hierarchical models: transistor (Spice level), structural (low level), behavioral (intermediate) and high level (ESL or Specification). To perform this, we used concurrently bottom-up and top-down approaches which allow separating significant parameters from the others.

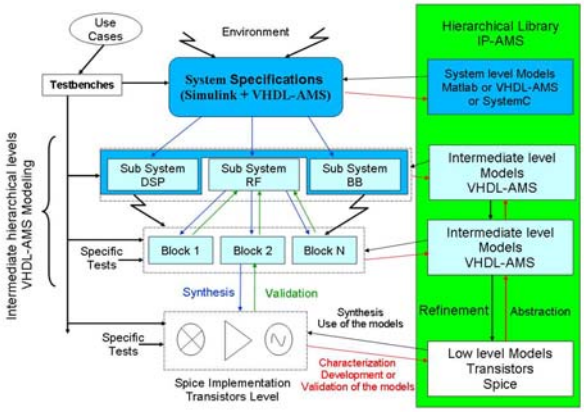


**Figure 2:** Methodology

## 3. BT architecture

To illustrate our methodology, we have chosen Bluetooth and BT over UWB (Ultra Wide Band) standards as example. Bluetooth is the technology that dominates the WPAN arena, offering low cost and low data rates communications. The last Bluetooth Specification [1], which was released by the Bluetooth SIG [2] in November 2004, introduces an Enhanced Data Rate mode that improves the data rate from 1 Mbps to 3 Mbps. Bluetooth uses a slotted protocol with a *frequency hopping spread spectrum (FHSS)* technique in the ISM frequency band (2.402 GHz – 2.483 GHz), which is unlicensed in most of the countries. A total of 79 channels of 1 MHz width are defined, where the data rates goes from 1 Mbps (*Gaussian Frequency Shift Keying (GFSK)* modulation) to 3 Mbps (*8-Differential Phase Shift Keying (8DPSK)*). The FHSS sequence is obtained by derivating the master clock. The transmission channel changes 1600 times per second, therefore time is divided into 625 µs slots using a *Time Division-Multiplexing (TDM)* scheme. Figure 3 illustrates the architecture of the BT transceiver.

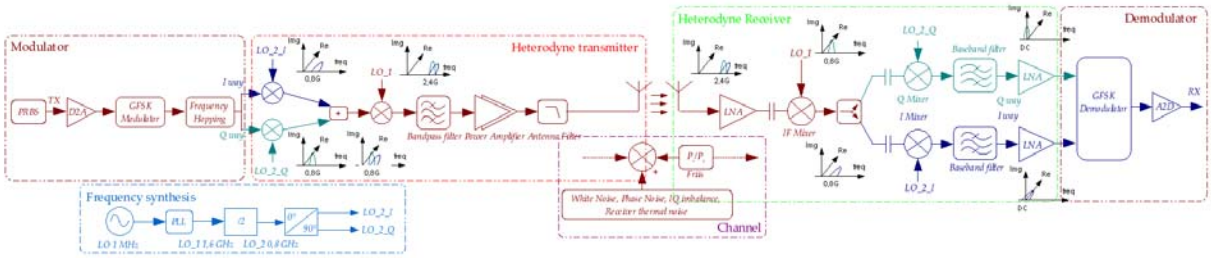


**Figure 3:** BT transceiver architecture

## 4. BT over UWB (BT3.0)

Contrary to Bluetooth, the Wimedia [3] standard only defines a MAC and a PHY layer for the UWB technology. Bluetooth, which whole protocol stack is defined, will use Wimedia UWB to provide the Bluetooth technology the following advantages:

- High data – low power rate communications.
- Efficient access to the medium.
- Quality of Service (QoS).

To do so, a convergence layer needs to be defined to allow the upper layer of the Bluetooth stack to use the Wimedia MAC and PHY layers.

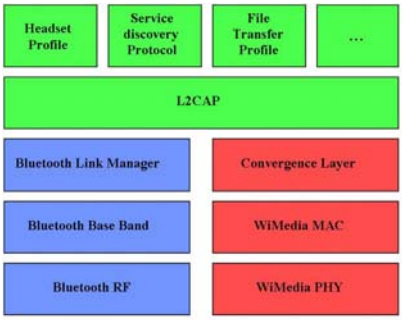


**Figure 4:** Reference Model (BT+UWB Special Group)

On figure 4, in red is shown the UWB specific layers, in blue the Bluetooth layers and in green the existing BT layers that need to be modified to enable UWB communications. Consequently, a Bluetooth device that implements both PHY and Baseband/MAC layers can choose the BT PHY to perform low data rate application) or the UWB PHY to rapidly transfer large video or audio files.

## 5. Results

A SystemC simulator has been developed to implement the BToUWB standard at the MAC level. This simulator analyses the performances of the Beaconing and estimates the power consumption. The Wimedia SystemC simulator is illustrated on figure 5.

At lower level, the complete structure of the Bluetooth transceiver has been modeled at different levels using Matlab (Simulink) and VHDL-AMS (ADMS). One critical part of this system is the frequency generator (PLL) [4]. On figure 6, we compare different simulated results versus an experimental measurement.

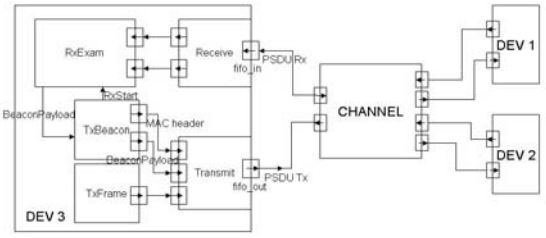


**Figure 5:** Wimedia SystemC simulator structure

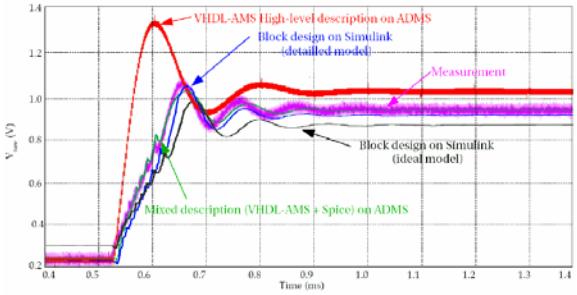


**Figure 6:** Comparison of different hierarchical levels

## 6. Conclusion

We have developed a multi-engine, multi-domain and hierarchical framework for simulating communicating objects. More results will be presented on the university booth.

## 7. References


[1] Bluetooth SIG, "Specification of the Bluetooth System - Core" Core Specification v2.0 + EDR, Nov. 2004, https://www.bluetooth.org/spec/

[2] http://www.bluetooth.com

[3] ECMA International, Standard ECMA-368, "High Rate Ultra Wideband PHY and MAC Standard" Dec 2005, http://www.ecma-international.org/publications/standards/Ecma-368.htm

[4] B. Nicolle, W. Tatinian, J. Oudinot & G. Jacquemod, "Hierarchical modeling of a fractional PLL", PATMOS, Montpeiller 2006, pp. 450-457


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