

UT Mixed-Signal Simulator

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Abstract

UT Mixed-Signal Simulator is a mixed-signal, mixed-domain, and mixed-language design environment which supports VHDL-AMS 1999, VHDL-2002, Verilog 2001, SystemVerilog 2005 assertions, and SystemC 2005.

1. Introduction

More and more designers are moving to system level design in which design description and simulation are at the system level. For this, designers need a framework and an environment to model different parts of a system with different domains in a unified method. This way, they will be able to examine the interaction between all parts of the system during the design process.

Complex systems like SoCs may consist of analog, digital, mechanical, thermal, and parts from other domains. These parts should be able to work together harmoniously. Therefore, it is required that an environment that provides a multi domain design and simulation environment be used for developing such systems. This work focuses on this multi domain simulation environment.

In this project we have developed an environment for mixed-signal, mixed-domain, and mixed-language design and simulation. The simulator supports three standard HDLs (VHDL-2002 [1], Verilog 2001 [3] and SystemC 2005 [4]). It also supports VHDL-AMS 1999 [2] for mixed-signal and mixed-domain simulation. The simulation environment enables designers to develop their designs that are a combination of three languages (i.e., VHDL-AMS, Verilog SystemC). In addition, it provides assertion verification environment supporting the SystemVerilog 2005 [5] design language. Furthermore, the simulator provides several code and functional coverage measurements that work with all supported languages.

The environment includes a waveform viewer and an editor. The waveform editor is useful for constructing and editing waveforms in order to generate testbenches visually. All the above components are integrated in our graphical environment that runs under Microsoft Windows XP. There is a set of more than 25,000 VHDL, Verilog and also SystemC testcases that we used for testing the tool. The environment consists of these major parts: Analyzers, Elaborator, Simulator, Wave Viewer, and GUI.

Section 2 of this project description presents our analyzers and the elaborator. Section 3 demonstrates the simulator and its kernel. Section 4 describes the graphical user interface of the simulator. Section 5 is the conclusion of this paper. References come last in this project description.

2. Analyzers and Elaborator

TOSIF is an object oriented intermediate format basically designed to support VHDL (IEEE Std 1076-1993, IEEE Std 1076-2002), VHDL-AMS analog extensions to VHDL (IEEE Std 1076.1-1999), Verilog (IEEE Std 1364-1995, IEEE Std 1364-2001) and SystemC (OSCI version 2.1, now IEEE Std 1666-2005), and SystemVerilog (IEEE Std 1800-2005) assertions. As shown in Figure 1, the analyzers are applications that generate TOSIF intermediate format from input source files.

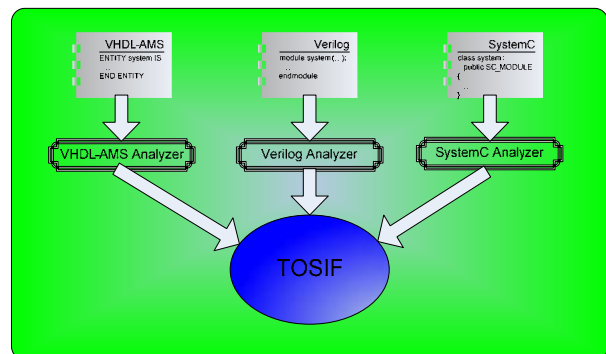


Figure 1: Analyzers and TOSIF

After analyzing a source file and creating a library unit in TOSIF, several elaboration tasks should be done on this library unit to prepare it for back-end applications such as the simulator. Such tasks are: removing the design hierarchy and flattening the design, applying design configurations, replacing static expressions with their explicit values, etc.

3. Simulator

Typically, a simulation process begins with a design given in an HDL. This design should be converted to an intermediate format (IF) that will be used by the simulator that uses this intermediate format as its starting point. In this work, this intermediate format is TOSIF. Next, the simulator reads this IF and generates its internal data structure, called SIRE. Simulation begins after this phase. As shown in Figure 2, inputs and outputs of the simulator are as follow:

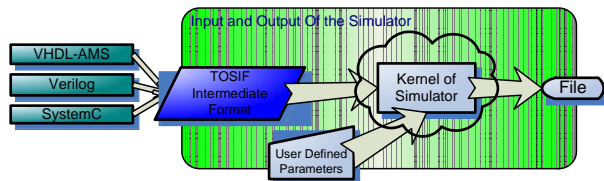


Figure 2: Input and Output of the simulator

- TOSIF is the memory representation of a design. Analyzers and elaborators are intended to generate TOSIF. The TOSIF structure is traversed to generate the simulator's internal data structure.
- The outputs of the simulator are two files: one in VCD format and another is our internal wave file format.
- In our simulator, some parameters are set by the users. These parameters use to configure the functionality of our simulation engine.

The kernel of the simulator is the simulation manager that manages the functionality of the mixed signal simulator. As shown in Figure 3, the kernel consists of several major parts such as SIRE [9] as the simulation internal intermediate format, execution unit, SIRE handler, event handler [6] [7] [8], generator unit and analog solver [6] [7] [8], and several utilities such as DAE solver, expression evaluator, memory manager, log file generator, test environment and the VCD file creator. It also provides several interfaces for other tools such as the elaborator and wave viewer.

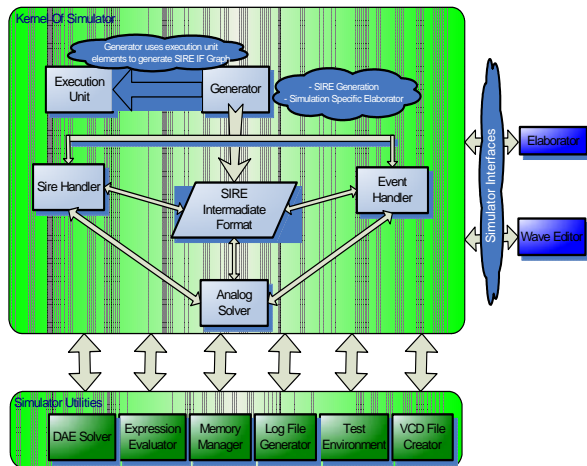


Figure 3: Different parts of the simulator kernel and the simulator utilities

4. GUI

Our graphical user interface provides an environment for SystemC design and verification. It consists of the following parts:

- 1- Design manager: provides facilities for managing workspaces and projects.
- 2- Text editor: enables users to edit their VHDL-AMS, Verilog and SystemC source files. It has common edit features as well as syntax highlighting for all the languages.
- 3- Waveform viewer and editor: that is used for viewing results of simulation and also editing waveforms for

testbench generation. The waveform viewer and editor support standard VCD format and its own binary format. The viewer has common features such as zoom, cursor, and changing visual signal attributes such as color and data format. The editor is used for testbench generation. It supports different data types of the languages and can be used to edit a single or repeated value in different ways. The editor can generate VHDL, Verilog and SystemC testbenches.

5. Conclusion

In this project, we have developed an environment that provides a multi domain simulation environment. It is a mixed-signal, mixed-domain, and mixed-language design environment that supports VHDL-AMS 1999, VHDL-2002, Verilog 2001, SystemVerilog 2005 assertions, and SystemC 2005.

6. References

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- [2] IEEE Std 1076.1-1999, IEEE Standard VHDL Analog and Mixed-Signal Extensions, 1999.
- [3] IEEE Std 1364-2001 IEEE Standard Verilog Hardware Description Language, 2001.
- [4] IEEE Std 1666-2005 IEEE Standard SystemC Language Reference Manual, 2005.
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