

# INTEREST (Integrating European Embedded Systems Tools)

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## Abstract

The project INTEREST aims at overcoming the current lack of integration and interoperability of tools for developing embedded systems software. Special focus is on performance, memory and timing.

## 1. Introduction

The project INTEREST is an FP6 STREP that has been launched in 2006. INTEREST aims at overcoming the current lack of integration and interoperability of tools for developing Embedded Systems software, with special focus on *automotive* and *aerospace* applications.

The partners in the project comprise a unique group of European tool vendors that jointly address the Embedded Systems design flow. The following capabilities are targeted:

- Mapping of a logical architecture, i.e. the structure of the control-algorithms, to a technical architecture,
- Analysis of Timing-related objectives for System and Nodes
- Tool integration along the “V” development cycle, spanning all the analysis, system design, module design, implementation (including certified code generation), functional testing, module testing, system testing and requirements testing

It will achieve its aims by creating techniques for improved interoperability (the INTEREST development framework) among European embedded systems design, code generation, and verification COTS tools, which could not have previously been achieved:

- SCADÉ from ESTEREL TECHNOLOGIES
- ASCET and INTECRIO from ETAS
- DESIGNER Pro from DECOMSYS,
- Dependable COTS code (such as UNIS hardware abstraction layer COTS)

The project will develop novel techniques for system-level and node-level analysis of non-functional properties, such as *Worst Case Execution Timing*, *Stack usage* and *Schedulability analysis*.

- These Analysis tools from ABSINT, EVIDENCE and SYMTAVISION will be then integrated into the INTEREST development framework.

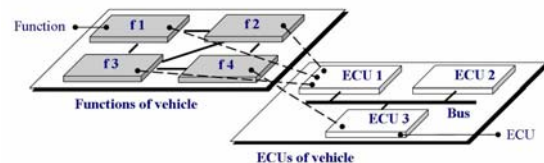
Demonstration within the Aerospace and Automotive Validators will show the clear path to the overarching objectives:

- significant time gain in timing analysis
- significant gain in mapping time and significant improvement of mapping quality
- improved resource usage through automatic schedule optimization.

## 2. Approach

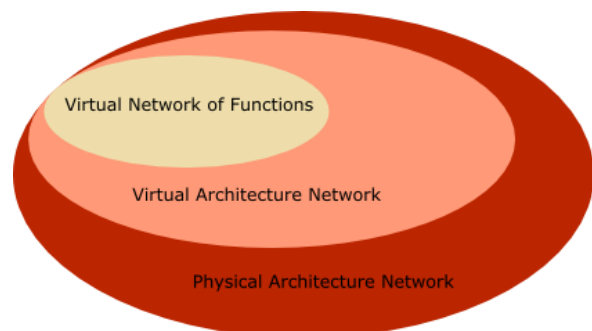
One of the main design challenges in complex embedded real-time system design consists of mapping a logical architecture [1], i.e. the structure of the control-algorithms, implemented by a set of application software modules to a technical architecture, i.e. the nodes and the network elements as well as the basic software modules, under typical real-time and resource consumption limitations.

For automotive systems, this mapping is shown in **Figure 1**. For aerospace and transportation systems, additional redundancies are being added to this representation.



**Figure 1:** Mapping of a Logical Architecture (Functions of System) to a Technical Architecture (ECUs of System)

Doing this mapping appropriately involves several integration steps. For each integration step, there exists an own model. These models can be arranged in shells, going from a pure functional model to the integrated physical system. These shells are shown in **Figure 2**.



**Figure 2:** INTEREST Shells

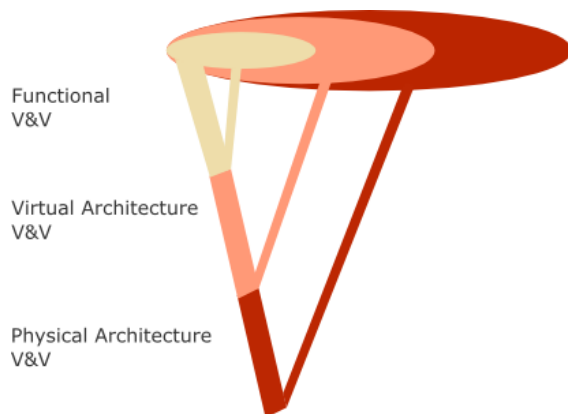
In the early integration steps logical components are mapped to the virtual components. Having the abstract knowledge, code-generation applied to the functional models will yield source-code which can be analysed by Worst-Case Execution Timing (WCET) and stack-estimation tools.

Knowledge of the timing attributes of the code can be assumptions and constrains of the abstract models and appropriate schedulability analysis is performed. It is to be noted that for aerospace applications, the synchronous/reactive assumptions are key in ensuring compliance of the generated code to safety objectives, such as the one of DO-178B standard in aerospace, or IEC 61508 standard for automotive, transportation and industrial systems.

Furthermore, since no physical architecture has been implemented up to this point, the cost for modification is low. The virtual architecture can thus be modified to meet timing constraints, and also optimized towards minimum cost, maximum extensibility and other goals

The physical architecture network will assign the virtually integrated logical architecture with a real physical architecture. Analysis on the real system will reveal whether all virtual obtained results of the synchronous/reactive assumption still holds in a real system.

Applying this shell approach to the classical V-Cycle in the design of embedded systems as shown in **Figure 3**, the designer obtains an earlier feedback w.r.t. verification & validation (V&V)[2]. While the inner- and the outer Vs are well understood, the middle V, i.e. the virtual architecture V&V has to be investigated and validated further.



**Figure 2:** Coarse Grain View of Embedded V&V Activities

A second layer of structuring is the scope of an architecture entity. From the INTEREST project point of view, there exist 3 suitable scopes:

- the entire system,
- one node,
- and one component.

On each architectural level and for each scope, the INTEREST project will comprise structural and methodological aspects.

- **Structural:** appropriate performance/timing models will be introduced on each architecture level and for each scope.
- **Methodological:** Once the structural foundations have been established, they shall be applied both for estimation and optimization while transitioning from the functional V&V to the virtual architecture V&V, and for verification while transitioning from the virtual architecture V&V to the physical architecture V&V.

The INTEREST project will address key customer requirements, including accuracy, coverage, speed, ease of use and composability.

To maximize applicability and potential for dissemination, INTEREST will consider standards for system integration processes (such as AUTOSAR and IMA, and the SPEEDS IP FP6 project proposal), as well as communication and RTOS standards (CAN, TTP, FlexRay, OSEK, ARINC 653, AUTOSAR/RTE etc.).

### 3. Results and Measure

The overarching objectives of INTEREST are to reduce the time for the integrated development of embedded systems and the cost of development of these systems.

In a period of five years after project start, we expect to achieve a reduction of 80% or more of the cost of performing mapping and timing analysis tasks within a typical embedded systems design project.

### 5. References

- [1] Schüffele, J., Zurawka, T., *Automotive Software Engineering*. SAE-International, Warrendale, 2005
- [2] Schiele et al.: *Rapid Design Exploration for Safety Critical Automotive Systems*, *Proceedings of the 1st Embedded Real-Time System Symposium, Toulouse 2002*

### Acknowledgement

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