GAUT – High Level Synthesis – From C to RTL

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Abstract

GAUT, A HLS tool, extracts a CDFG from a C function and selects, allocates, assigns and schedules RTL hardware ressources. GAUT generates a pipelined architecture composed of processing, memory, communication and multiplexing units as well as a GALS/LIS interface.

1. SoCs are complex ICs

In the SoCs context, the traditional IC design methodology relying on EDA tools used in a two stages design flow -a VHDL/Verilog RTL specification, followed by logical and physical synthesis- is no more suitable. However, the increasing complexity and the data rates of DSP applications requires efficient hardware implementations like dedicated accelerators or coprocessors. Thus actual SoC embedded DSP cores need new ESL level tools in order to raise the specification abstraction level up to the « algorithmic one ».

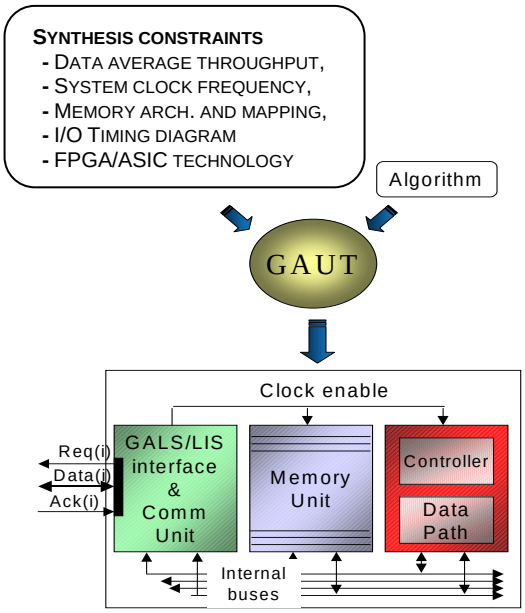
The function is the added-value

Algorithmic descriptions enable an IC designer to focus on functionality and target performances rather than debugging RTL. Designers spend more time exploring the design space with multiple "what if" scenarios. They obtain a range of implementation alternatives, from which they select the architecture providing the best power/speed/gate count trade-off.

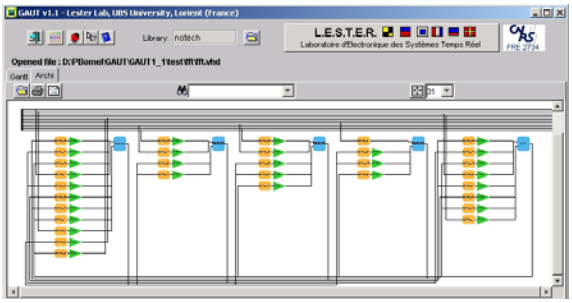
From C to ICs: GAUT

CatapultC from Mentor Graphics or Agility Compiler from Celoxica are EDA software tools enabling to capture such C-based algorithmic design entries and synthesize them into an equivalent RTL specification. GAUT is an academic HLS tool dedicated to DSP applications. Starting from a pure C function GAUT extracts the potential parallelism before selecting, allocating, assigning, and scheduling hardware operations. GAUT generates a potentially pipelined architecture composed of a processing unit, a memory unit, a communication and multiplexing unit and a GALS/LIS interface.

GAUT, a HLS tool



GAUT generates an IEEE P1076 VHDL file. The VHDL file is an input for commercial, off the shelf, logical synthesis tools like ISE/Foundation from Xilinx, Quartus from Altera or Design Compiler from Synopsys. GAUT generates a SystemC Cycle Accurate CA simulation model which is SystemC 2.1 compliant. GAUT generates a VHDL test-bench and is seamlessly interfaced with Modelsim from Mentor Graphics. VCD traces can be displayed with gtkwave.



Function Capture & Graphical User Interface

GAUT is currently supported on Linux and Windows. A syntax-guided text editor allows the designer to capture and analyze DSP algorithms. An output of the analysis is a graphical view of the data flow graph that expresses all the potential parallelism of the code. The outputs of the synthesis are the RTL file and a GANTT view of hardware resources. There is currently an architectural view of the processing unit extracted from the RTL file.

IC hardware interfaces

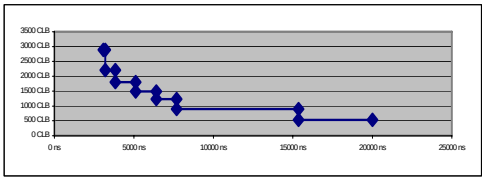
GAUT generates protocol specific interfaces. This enables to execute the synthesized DSP applications in a mixed hardware/software system. This approach has been validated with the PALMYRE platform -based on C6x from TI and Virtex from Xilinx- allowing to build various communication topologies.

Field testing

GAUT ICs are tested with the PALMYRE platform in various FPGAs contexts. FPGAs are stimulated by test pattern generators and results collected with logic analyzers. Mixed software/hardware configurations also allow to connect DSPs to/from FPGAs and deliver/collect data on the field without the need for heavy instrumentation. Hardware and software interfaces/libraries have been developed to ease interconnect of processes at C code level.

The PALMYRE platform

2. Results



This curve illustrates the impact of the time constraint (ns) in term of VirtexE CLBs for a 256 points FFT.

Relative complexities of the algorithmic and RTL abstraction level specifications for a Virtex target are illustrated bellow.

Function	*Algo level*	*RTL level*
8st. Viterbi	68 lines	4155 lines
FIR 1024	35	8889
LMS 512	47	9429
LMS 1024	47	17827

3. Références

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