Embedded Tutorial 1:
Future Directions in Clocking Multi-Ghz Systems

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This tutorial addresses the problems and possible solutions of clocking digital systems operating at multi-GHz frequencies. The first part of the tutorial will address techniques for managing clock uncertainties and clock power in synchronous circuits. There are two trends that are disturbing: (a) the power taken by the clock distribution network and clocked storage elements (flip-flops and latches) is increasing relatively to the rest of the logic, (b) clock uncertainties are taking a significant portion of the cycle away from useful logic operations. There are no radical solutions in sight. We present the ways of designing clock storage elements that are capable of absorbing significant portion of clock uncertainties and passing delay from one logic stage to the other. At multi-GHz frequencies of operation it will be difficult to precisely control the timing boundaries between the logic stages. Thus the ability to extend the operation into the time period allocated for the next pipeline stage is important. This is known as time borrowing. Also, the ability to incorporate logic into the clocked storage elements is of critical importance given that the number of logic stages in a pipeline running at multi-GHz frequencies, is decreasing to less than ten.

For achieving low power we present clocked storage elements with various features that are suitable to low power operation. Those are: selective clocking, conditional data capture, conditional precharge etc. We show a new family of dual-edge triggered clocked storage elements that are comparable in power and speed to their single-edge triggered counterparts. By synchronizing the events on every transition of the clock, instead of only on one of the two, we can run the system at half of the clock frequency effectively reducing the power spent on the clock subsystem in half.

We are aware that running a billion-transistor chip synchronously would be very difficult. Therefore, we believe that the boundaries between the pipeline stages in a synchronous system running at multi-GHz frequencies will start to blur with clocked storage elements serving only the purpose of synchronization between the stages – not latching the data. We also believe the future chips will be clocked synchronously only in limited domains while the communication between the domains will be asynchronous.

The second part of the tutorial will address the design of such self-timed systems in which local handshaking is used to provide the necessary synchronization and sequencing of operations. The possible solutions range from completely asynchronous circuits to globally asynchronous locally synchronous (GALS) systems, which use local clocks. The International Technology Roadmap for Semiconductors predicts that such solutions will be needed in the future because global synchronization becomes technically infeasible and because the CMOS transistor becomes subject to ever-larger statistical variations in its behavior.

Although asynchronous design largely avoids these problems, is by no means straightforward. In addition to issues like CAD tools and testability (which are being addressed), a synchronous design engineer who approaches asynchronous design for the first time will face several challenges. The first big hurdle to be cleared is that of mindset — asynchronous design requires a different mental approach from that normally employed in clocked design. Attempts to take an existing clocked system, strip out the clock and simply replace it with asynchronous handshakes are doomed to disappoint. Another hurdle is that of circuit design methodology - the literature presents an apparent plethora of disparate approaches.

The tutorial will address these issues, present some fundamental concepts, and emphasize the common ground. Finally the tutorial will briefly touch upon the current state of the art in CAD tools and circuit design.

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