Oversampled Gain-Boosting

Omid Oliaei

Motorola Labs, Communications Research Lab, 1301 E. Algonquin, Schaumburg, IL 60196-1095
Email: Omid.Oliaei@motorola.com

ABSTRACT
A dynamic gain-enhancement technique suitable for low-voltage low-power oversampling circuits, particularly sigma-delta converters, is presented. This method makes use of a discrete-time integrator to improve gradually the output resistance of the main amplifier over successive clocks.

Categories and Subject Descriptors
B.7.1 [Hardware]: Integrated Circuits

General Terms
Circuit Design

Keywords
Switched-Capacitor, MOS amplifier, bootstrapping, ADC, DAC, sigma-delta, gain boosting, gain enhancement, OTA.

1. INTRODUCTION
Accuracy of various functions realized by SC-circuits largely depends on the performance of operational amplifiers embedded in their structure. DC-gain is an important parameter for amplifiers specially in high-precision applications. Among numerous gain-enhancement techniques proposed for MOS amplifiers bootstrapping presents attractive features in terms of stability and speed [1], [2]. This technique is usually applied to single-stage amplifiers with a cascode output, Fig.1-a. The basic idea behind the gain-boosting technique is to maintain the drain voltage of transistor N1 at $V_d=V_r$ through the local feedback created by the additional amplifier. Consequently, the output resistance of the circuit is multiplied by the gain of the supplementary amplifier, *A*. A simple implementation of the gain-boosting technique is the regulated cascode [3], Fig.1-b. Unfortunately, this circuit is not suitable for low-voltage designs because V_d is dictated by Nr instead of N1. This clearly limits the voltage swing at the output. Active-bootstrapped gain-enhancement [4] is a similar technique proposed for two-stage amplifiers, Fig.1-c. This technique is very attractive for low-voltage operation because a high gain is achieved without stacking transistors in the output branch or even sacrificing the circuit bandwidth [5].

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Here, we present a gain-boosting technique suitable for oversampling circuits, specifically sigma-delta modulators. This technique exploits oversampling to enhance the effective DC-gain of the amplifier embedded in a SC-circuit. This method enables a regulated cascode to achieve the output swing of a simple cascode amplifier. Alternatively, it improves the output resistance of a two-stage amplifier without calling for an additional amplifier.

2. OVERSAMPLED GAIN-ENHANCEMENT
The principle of oversampled gain-boosting technique is illustrated in Fig.2. Compared with the structure in Fig.1-a, the amplifier has been replaced with a unity-gain discrete-time integrator. Again, the integrator creates a local feedback which seeks to maintain V_d close to V_r. However, since the integrator operates in discrete time-intervals, the feedback loop needs several clock periods in order to damp out the voltage variations at node X. From this explanation it becomes clear that the circuit accomplishes its task of gain-enhancement only if disturbances inflicted to node X occur at a slower rate than the clock frequency. This is obviously the case only for oversampled systems.

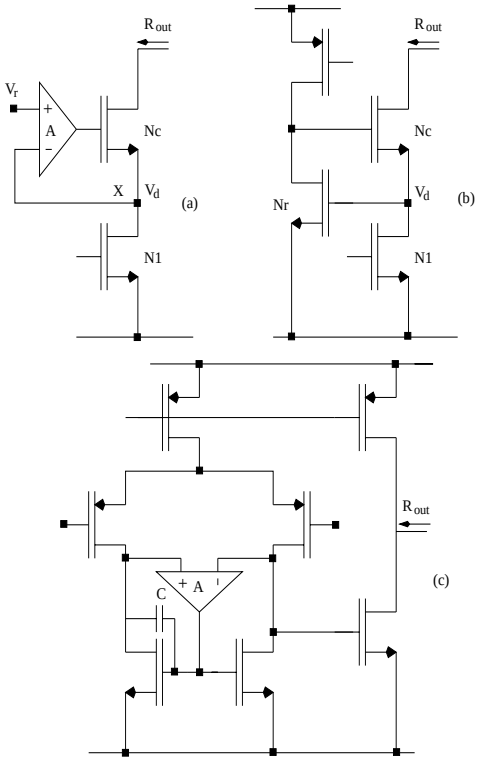

Figure 1. a) Basic gain-boosting technique, b) regulated cascode stage, c) active-bootstrapping.

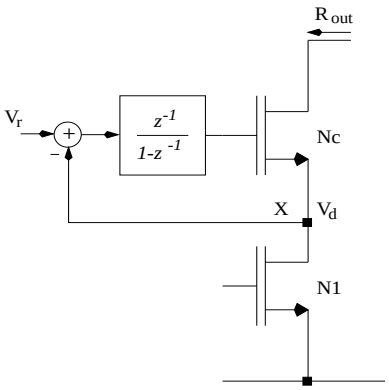

Figure 2. Basic oversampled gain-enhancement technique.

The discrete-time operation of the circuit is best described in the *z*-domain by writing the loop equation:

$$(V_r - V_d)\left(\frac{z^{-1}}{1-z^{-1}}\right) - V_{gsc} = V_d \tag{1}$$

where V_{gsc} is the gate-source voltage of the cascode device, Nc. This can be simplified as:

$$V_d = V_r z^{-1} - V_{gsc}(1-z^{-1}) \tag{2}$$

At low frequency, i.e., $z^{-1} \rightarrow 1$, the voltage V_d approaches V_r. In other words, any voltage variation at X vanishes after a few clock periods. To calculate the output resistance, the transistors are replaced with their small-signal representation and V_r is set to zero, Fig.3. In this case, we have:

$$g_{mc}\left(\frac{-z^{-1}}{1-z^{-1}} - 1\right)v_d + g_{dc}(v_s - v_d) = g_d v_d = i_s \tag{3}$$

From this, the output resistance is obtained as:

$$R_{out}(z) = \frac{1}{g_d} A_c \frac{1 - z^{-1}/A_b}{1 - z^{-1}} \tag{4}$$

where we have defined:

$$A_b = \frac{g_d + g_{dc} + g_{mc}}{g_d + g_{dc}} \tag{5}$$

$$A_c = \frac{g_d + g_{dc} + g_{mc}}{g_{dc}} \tag{6}$$

A_b and A_c designate the boosting and cascode gains, respectively. It is interesting to note that the result in (4) provides the output resistance in the *z*-domain. According to (4), at low frequency the output resistance, $R_{out,}$ tends to infinity. In fact, if a voltage step is applied to the output, the current i_s will tend to zero after a few clock periods.

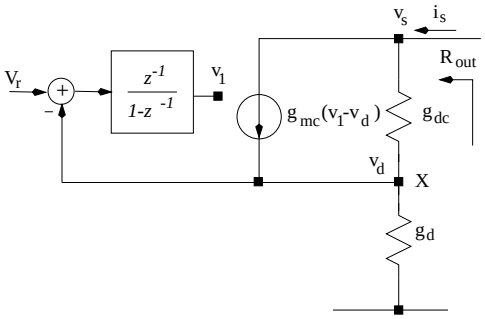

Figure 3. Equivalent small-signal circuit of Fig.2.

However, in a practical implementation the integrator has a finite DC-gain which limits the output resistance of the circuit. Practical implementations are the subject of the two next sections.

3. OVERSAMPLED REGULATED CASCODE

A practical oversampled regulated cascode stage is shown in Fig.4. Transistors Nr and Pr operate together as a simple amplifier. The switches and capacitors along with the amplifier constitute a classical lossless SC-integrator [6]. The circuit principally makes use of the same clocks used by the entire system in which this amplifier is embedded. During phase $\phi 1$ the voltage at node X is sampled and during $\phi 2$ it is integrated. The recursion equation describing the circuit operation is written as:

$$C[V_r - V_d(n-1)] + C[V_1(n-1) - V_g(n-1)] =$$

$$C[V_b - V_g(n)] + C[V_1(n) - V_g(n)] \tag{7}$$

At steady-state these voltages settle to their final value: $V_1(n)=V_1(n\text{-}1)$ and $V_g(n)=V_g(n\text{-}1)$. So:

$$V_d = V_r - V_b + V_g \tag{8}$$

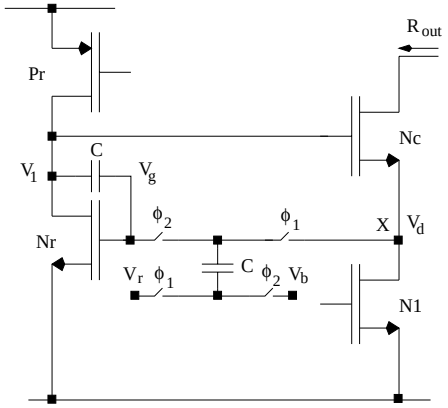

Figure 4. Oversampled regulated cascode.

Choosing V_b=V_g, the drain voltage of N1, V_d, will approach V_r if enough time is given to the system. Therefore, the drain voltage of N1 can be set at a voltage just high enough to ensure the saturation of N1. The voltage V_b can easily be generated by a branch composed of transistors identical to Nr and Pr. As pointed out earlier, finite gain of the simple amplifier composed of Nr and Pr causes the integrator to be leaky. The gain of the regulating amplifier is:

$$A_r = \frac{g_{mr}}{g_{dnr} + g_{dpr}} \tag{9}$$

where g_{mr}, g_{dnr} and g_{dpr} are the transconductance of Nr, gate-drain conductance of Nr and gate-drain conductance of Pr, respectively. Taking into account the amplifier gain, the integrator transfer function becomes, [6]:

$$H(z) = \frac{\left[1 + \frac{2}{A_r}\right] z^{-1}}{1 - \left[1 - \frac{1}{A_r}\right] z^{-1}} \tag{10}$$

Substituting the above transfer function in relation (3) instead of an ideal transfer function yields:

$$R_{out}(z) \approx \frac{1}{g_d} A_c \frac{1 - \left[\frac{1}{A_b} - \frac{3}{A_r}\right] z^{-1}}{1 - \left[1 - \frac{1}{A_r}\right] z^{-1}} \tag{11}$$

At low frequency the output resistance tends to:

$$R_{out} \approx \frac{1}{g_d} A_c A_r \tag{12}$$

which is exactly the output resistance of a classical regulated-cascode.

Charge injection and parasitic gate-drain capacitance of Nr are two other sources of non-ideality. Since the voltage at node X is almost constant, charge injection gives merely rise to an offset voltage term in equation (8). The parasitic gate-drain capacitance of Nr makes the gain of the integrator different from unity. This effect is negligible if C_{gd} is kept much smaller than C.

It is well-known that the cascode transistor, Nc, doesn't contribute to the total output noise of the cascode amplifier [7]. In this regard, sampled noise generated in the integrator structure only adds up to the noise of the cascode transistor and thereby doesn't increase the output noise. Therefore, the capacitors C can be quite small since the limiting factors in their downsizing are only the offset voltage due to charge injection, matching and the gate-drain parasitic.

Study of the circuit stability requires a small-signal analysis for each clock phase. On phase ϕ1 node X is loaded by a capacitor C. This capacitor actually replaces the gate-source capacitance which existed in the case of the classical regulated cascode. If the cascode stage is placed in the signal path, the node X creates a non-dominant pole. Hence, the phase margin of the main amplifier may decrease if C is too large. On phase ϕ2, the sampling capacitor C is disconnected from this node and it doesn't affect the phase margin. On the other hand, the gate of the cascode transistor, Nc, is driven on both phases by the output of the integrator which is a low-impedance node. Therefore, operation of the regulating amplifier in the discrete-time domain doesn't compromise the circuit stability. The regulating integrator is desired to settle as fast as possible during ϕ2 because its incomplete settling translates into a gain error [6] and thereby makes the gain-boosting less efficient. Fortunately, the simple structure of the integrator and its small capacitive load allow for a fast settling without drawing an excessive bias current.

From relations (4) and (11) it is apparent that the output resistance of a dynamic gain-enhanced circuit should exhibit a discrete damped exponential improvement over time. So it is expected that when a voltage step is applied to such a circuit, the current flowing through it should exponentially decrease. To demonstrate this transient response, a regulated cascode stage using dynamic gain-boosting for both PMOS and NMOS sides was simulated. The input current to the circuit after applying a 100 mV voltage step is shown in Fig.5. As expected the input current goes exponentially towards its final value of 0.35 nA. This represents an output resistance of 286 MΩ versus 4.35 MΩ obtained for the basic cascode stage without gain-boosting.

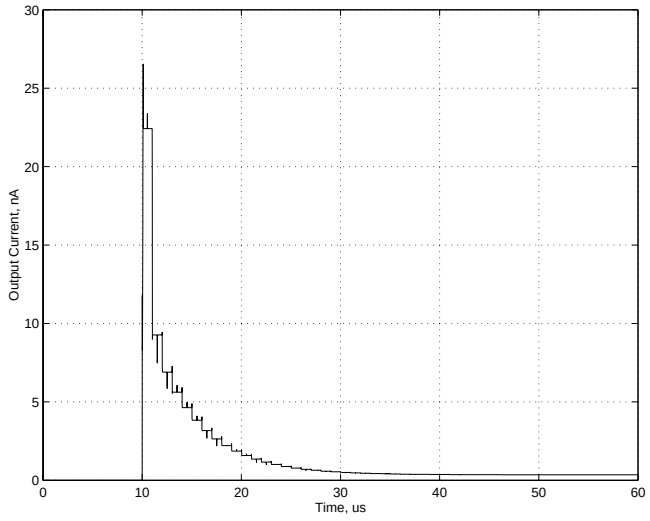

Figure 5. Transient current flowing into an oversampled regulated cascode in response to a 100 mV voltage step.

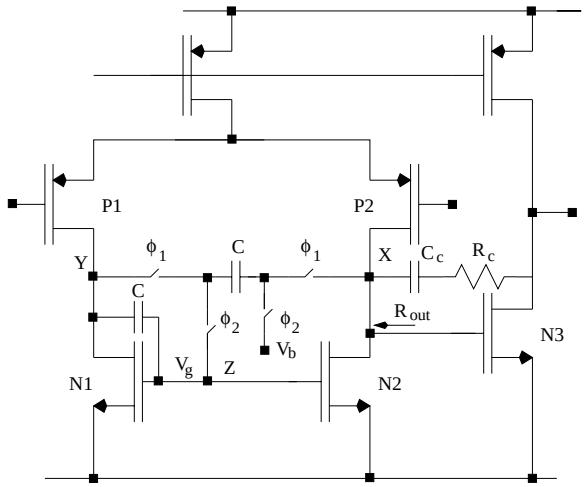

Figure 6. Oversampled active bootstrapping.

4. OVERSAMPLED ACTIVE BOOTSTRAPPING

The principle of oversampled gain-boosting can also be applied to the circuit of Fig.1-c. In this case, the amplifier A is removed and the capacitor C is served as integrating capacitor, Fig.6. The bias voltage V_b is set equal to the steady-state gate-source voltage of N1 and N2. Transistors N1 and P1 operate as an amplifier to form the integrator. The recursion equation for this circuit is written as:

$$C[V_x(n-1)-V_y(n-1)]+C[V_y(n-1)-V_g(n-1)]=$$

$$C[V_b(n)-V_g(n)]+C[V_y(n)-V_g(n)] \quad (13)$$

At steady-state we have: $V_g(n)=V_g(n-1)$ and $V_g(\infty)=V_b$, so: $V_y(\infty)=V_x(\infty)$. Note that this equality in the continuous-time circuit is established by means of an additional amplifier. For small-signal analysis, the equivalent-circuit in Fig.7 is used. The above equation is then modified as:

$$C[v_x(n-1)-v_y(n-1)]+C[v_y(n-1)-v_g(n-1)]=$$

$$C[-v_g(n)]+C[v_y(n)-v_g(n)] \quad (14)$$

In addition, we have two node equations:

$$g_{m1}v_g+g_{d1}v_y=0 \quad (15)$$

$$g_{m1}v_g+g_{d1}v_x=i_s \quad (16)$$

Taking z-transform from (14) and solving the resulted system of equations, we find:

$$R_{out}(z)=\left(\frac{1}{g_d}\right)\frac{1-\left(\frac{1}{2+A_b}\right)z^{-1}}{1-\left(\frac{1+A_b}{2+A_b}\right)z^{-1}} \quad (17)$$

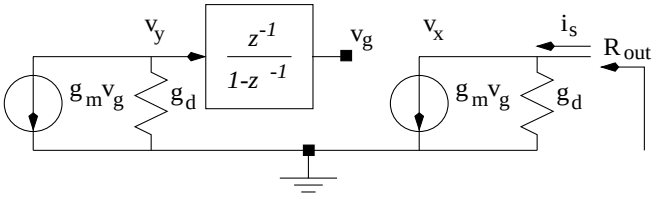

Figure 7. Small-signal equivalent circuit of Fig.6.

where $A_b=g_m/g_d$ and g_m and g_d are the transconductance and output conductance of transistors N1 and N2, respectively. The DC output resistance is obtained as:

$$R_{out}=(1+A_b)/g_d \quad (18)$$

It is seen that the output resistance of the amplifier is multiplied by the gain of the amplifier composed of N1 (N2) and P1 (P2). This corresponds exactly to the output resistance of the amplifier of Fig.1-c for $A=1$, [4], [5].

It is known that mismatch between N1 and N2 in a continuous-time active bootstrapping circuit may reduce the output resistance by an order of magnitude [4], [5]. To see the effect of mismatch in Fig.6, let's suppose that the g_m of N1 becomes $g_m+\Delta g_m$. To simplify the analysis, we suppose equal gate-source conductances, g_d, for N1 and N2. Repeating the analysis including this modification, the output resistance of the circuit becomes:

$$R_{out}(z)=\left(\frac{1}{g_d}\right)\frac{1+\left(\frac{1}{2+A_b}\right)\left(\frac{\Delta g_{m1}}{g_{m1}}\right)-\left(\frac{1}{2+A_b}\right)z^{-1}}{1+\left(\frac{A_b}{2+A_b}\right)\left(\frac{\Delta g_{m1}}{g_{m1}}\right)-\left(\frac{1+A_b}{2+A_b}\right)z^{-1}} \quad (19)$$

When $z^{-1}\rightarrow 1$, the output resistance tends to:

$$R_{out}=\left(\frac{1}{g_d}\right)\left(1+\frac{A_b}{1+\left(\frac{\Delta g_{m1}}{g_{m1}}\right)(2+A_b)}\right) \quad (20)$$

For 1% mismatch and $A_b=100$, the output resistance is divided by two. So, the effect of mismatch on the oversampled gain-bootstrapped circuit is not significant. The circuit can be conveniently designed using the approach described in [5]. Small-signal analysis of the circuit shows that the gain-bandwidth product is still given by: $GBW=g_{mp1,2}/C_c$ and using $R_c=g_{mn3}$ one of the zeros in the transfer function can be pushed to infinity. For $g_{mn3}>>g_{mn1,2}$ and $C_c>>C$ the non-dominant pole on phases $\phi1$ and $\phi2$ is:

$$s_{pnd}\big|_{\phi 1}=\frac{-1}{\frac{C}{g_{mn2}}\left(1+\frac{2C_1}{C}\right)+\frac{C_L}{g_{mn3}}} \quad (21)$$

$$s_{pnd}\big|_{\phi 2} = \frac{-1}{\frac{C}{g_{mn2}}\left(1+\frac{C_1}{C}\right)+\frac{C_L}{g_{mn3}}} \tag{22}$$

where C_1 is the parasitic capacitance at node Z and C_L the load capacitance at the amplifier out. It is seen that the dominant pole of the amplifier is not affected by the gain-boosting circuit. Since the load capacitance C_L is usually much larger than C, the non-dominant pole on both phases is approximately: $S_{pnd} \approx -g_{mn3}/C_L$ which is similar to the expression for the classical Miller amplifier. The second zero in the transfer function is given by:

$$s_z\big|_{\phi 1} = \frac{-2g_{mn2}}{C_1} \tag{23}$$

$$s_z\big|_{\phi 2} = \frac{-2g_{mn2}/C_1}{1+C_1/C} \tag{24}$$

The degrading effect of the left-hand zero on phase margin can be avoided if $g_{mn1,2}/C_1 >> GBW$. In practice this condition is easily fulfilled because C_1 is a parasitic much smaller than C_c. Therefore, it is possible to design the whole amplifier including the gain-boosting circuitry in such a way that its stability is ensured while its speed is preserved.

A second implementation of the oversampled active bootstrapping technique is shown in Fig.8. The left side of the gain-enhancement circuit implements an inverting integrator and the right-side a non-inverting integrator [8]. The output resistance of the circuit is again given by (17). Small-signal analysis of the circuit shows that the gain-bandwidth is still obtained from: $GBW = g_{mp1,2}/C_c$ and:

$$s_{pnd}\big|_{\phi 1} = \frac{-1}{\frac{C}{g_{mn2}}\left(1+\frac{2C_1}{C}\right)+\frac{C_L}{g_{mn3}}} \tag{25}$$

$$s_{pnd}\big|_{\phi 2} = \frac{-1}{\frac{C}{g_{mn2}}\left(3+\frac{C_1}{C}\right)+\frac{C_L}{g_{mn3}}} \tag{26}$$

$$s_z\big|_{\phi 1} = \frac{(-2g_{mn2})/C_1}{1+2C_1/C} \tag{27}$$

$$s_z\big|_{\phi 2} = \frac{-2g_{mn2}/C_1}{3+2C_1/C} \tag{28}$$

Compared with the first implementation, it is seen that the expressions are quite similar but the zeros and non-dominant poles occur at lower frequencies. It is worth noting that likewise the continuous-time bootstrapped circuit, the gain-enhancement circuitry doesn't lead to an increased amount of noise at the output.

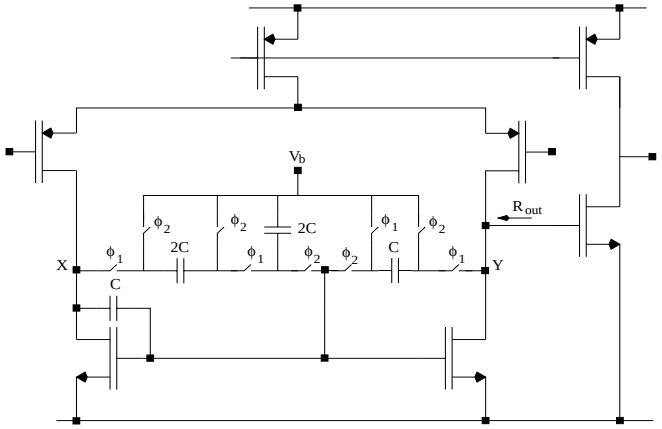

Figure 8. Alternative implementation of the oversampled active-bootstrapped amplifier.

5. SYSTEM APPLICATION

An important application of the oversampled gain-boosting technique is in sigma-delta converters. The finite DC-gain of the amplifier in a SC-integrator causes the integrator to be leaky. In fact, the transfer function of an SC-integrator using an amplifier with a DC-gain A_0 is, [6]:

$$H(z) = \frac{\frac{\alpha z^{-1}}{1+(\alpha+1)/A_0}}{1-\frac{1+1/A_0}{1+(\alpha+1)/A_0}z^{-1}} \tag{29}$$

where α is the gain of the integrator. Using the above relation, the noise and signal transfer functions of a second-order modulator using amplifiers with a nominal gain of $A_0=500$ were calculated and plotted in Fig.9. As expected a low DC-gain causes the quantization noise to flatten out at low frequency and thereby reduce the signal-to-noise ratio. The results of the previous sections demonstrate that applying the oversampled gain boosting to an amplifier with the DC-gain A_0 ideally leads to an amplifier with a z-domain gain as:

$$A_E(z) = A_0\frac{1-z^{-1}/A_b}{1-z^{-1}} \tag{30}$$

Including the finite gain of the boost amplifier, the expression for an oversampled regulated-cascode becomes:

$$A_E(z) = A_0\frac{1-(1/A_b-3/A_r)z^{-1}}{1-(1-1/A_r)z^{-1}} \tag{31}$$

Likewise for the oversampled active-bootstrapped:

$$A_E(z) = A_0\frac{1-\left(\frac{1}{2+A_r}\right)z^{-1}}{1-\left(\frac{1+A_r}{2+A_r}\right)z^{-1}} \tag{32}$$

Replacing A_0 in (29) with the expressions (31), (32) and (30) respectively, the curves (b), (c) and (d) in Fig.9 were resulted. It is seen that the gain-enhancement technique substantially reduces the quantization noise at low frequency and allows for a higher signal-to-noise ratio. The improvement even for $A_r=100$ is quite significant.

As a practical example, a second-order ΣΔ-modulator using fully-differential folded cascode amplifiers was considered. The first amplifier was then enhanced using the oversampled regulated cascode in Fig.4. The spectra in Fig.10, obtained from transistor-level simulations, show a higher rejection of quantization noise at low-frequency for the enhanced circuit which is an indication of higher effective DC-gain.

6. CONCLUSION

A low-cost gain-boosting technique exploiting the flexibility offered by oversampled systems was presented. Owing to the operation of the gain-enhancement circuitry in discrete time-intervals, the output resistance of the enhanced amplifier is described by an expression in the *z*-domain. This technique allows a regulated cascode stage to achieve the output swing of a plain cascode. Alternately, it increases the effective gain of a two-stage amplifier by an order of magnitude without incorporating an additional amplifier. Other variants of the proposed technique are likely conceivable. The presented approach pertains particularly to low-voltage low-power oversampling converters. The technique is also very efficient in terms of the occupied silicon area because it requires only small capacitors.

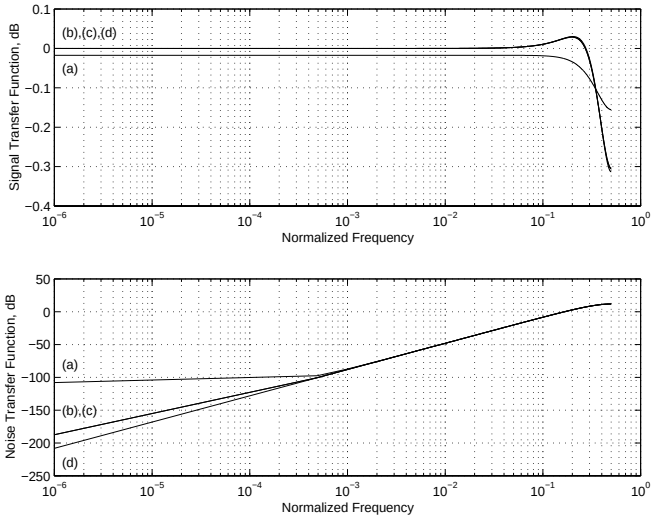

Figure 9. Signal transfer function and noise transfer function for: a) the basic amplifier with a gain of $A_0=500$, b) oversampled regulated cascode with $A_0=500$, $A_b=100$ and $A_r=100$, c) active-bootstrapped amplifier with the same values and d) enhanced amplifier with $A_0=500$, $A_b=100$ and $A_r \rightarrow \infty$.

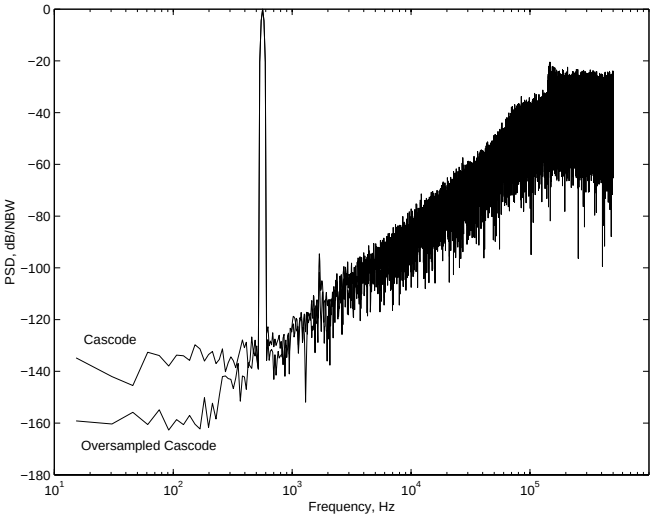

Figure 10. Comparison of the output spectra of a second-order ΣΔ-modulator using cascode and oversampled cascode amplifiers in the first integrator. Clock frequency is 1 MHz and the spectra were obtained from 64 k-point FFT's.

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