Closed-Loop Adaptive Voltage Scaling Controller For Standard-Cell ASICs

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ABSTRACT

The paper describes a closed-loop controller for adaptive voltage scaling (AVS) where the supply voltage to a standard-cell ASIC is dynamically adjusted to the minimum value required for the desired system speed. The controller includes a clock generator that provides a low-jitter clock to the ASIC at all steady-state operating points and through transients. To speed up the voltage transient response to step changes in clock frequency, the controller is based on a multiple-tap resettable delay line. A chip including the AVS controller and a dual 16-bit MAC application has been fabricated in a standard 0.5 μ CMOS process. The area taken by the AVS controller is 0.12 mm^2. Experimental results demonstrate operation over the application clock frequency range from 80 kHz to 20 MHz, and a 38 μs transient response for a step change in speed from standby to maximum throughput operation.

Categories and Subject Descriptors

B.7 [**Hardware**]: Integrated Circuits; B.5 [**Hardware**]: Register-Transfer-Level Implementation; B.8 [**Hardware**]: Performance and Reliability

General Terms

Design,Performance,Experimentation

Keywords

circuit design, design methodology, delay-line, low-power, energy-efficient, voltage scaling, standard-cell, DC-DC converter

1. INTRODUCTION

Adaptive (or dynamic) voltage scaling (AVS) has been proposed as an effective power management technique where the system clock frequency and the supply voltage are dynamically adjusted to meet the application throughput requirements [1]-[10]. Successful applications have included digital signal processing systems [1]-[5], I/O interface [6], and general-purpose microprocessors [7, 10].

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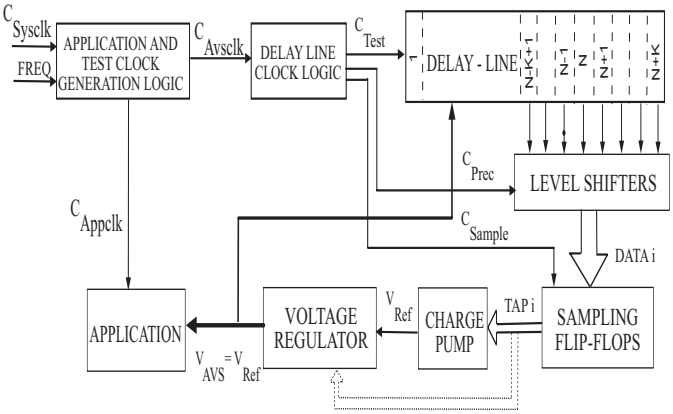

Figure 1: Simplified block diagram of the AVS scheme. Unless otherwise shown, all blocks use V_{DD} as the supply voltage.

At the system level, AVS requires a voltage/frequency scheduler that can intelligently vary the speed depending on the application requirements. At the hardware implementation level, the key AVS component is a controller that can automatically generate the minimum voltage required for the desired speed.

In an AVS controller, the reference circuit used to measure the gate delay is usually implemented using a chain of logic buffers operated as a ring oscillator whose frequency depends on the supply voltage [2, 10, 11, 12] or as a delay line speed detector [3, 5, 8]. In these approaches, the control loop design requires a careful compromise between the loop stability, dynamic response times, and the achievable range of operating clock frequencies [2, 10, 12] or multiple test clock cycles needed [3, 5]. Sliding-mode [11] and "bang-bang" [8] digital controllers have been proposed to achieve robust stability and fast transient responses.

The contribution of this paper is to describe a simple AVS controller where a multiple-tap resettable delay line is used as the reference circuit. It is shown how this design yields improved transient response by performing the delay test at one-half the system clock rate and by using the multiple taps to detect the error in the supply voltage. The controller is coupled to a clock generator that provides the test clock and the application system clock independently. This control scheme updates the low-jitter application clock seamlessly during step changes in clock frequency.

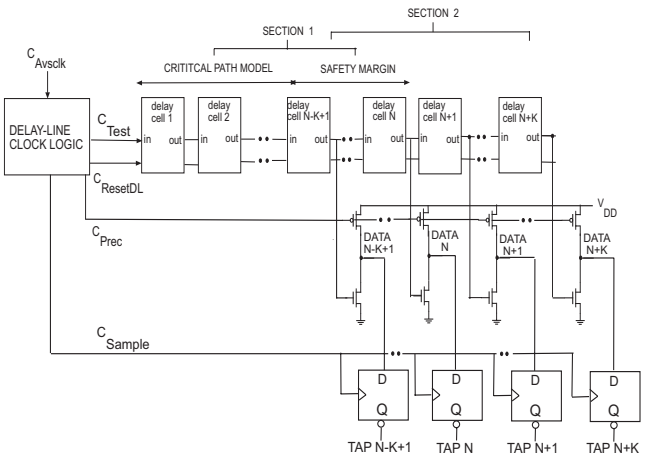

Figure 2: Block diagram of the resettable delay-line. Also shown are the level shifters to obtain logic signals compatible with the sampling flip-flops. The level shifters, flip-flops, and the delay line clock logic use constant V_{DD} as the supply voltage.

The paper is organized as follows. The proposed AVS controller is described in Section 2. Experimental results from a fabricated chip that combines the AVS controller and a dual 16-bit MAC are presented in Section 3 followed by conclusions in Section 4.

2. AVS CONTROLLER

Fig. 1 shows a simplified block diagram of the proposed AVS controller. It consists of:

(1) a resettable delay-line which operates from the adjustable supply voltage V_{AVS} and is driven by the test clock C_{Test}. In steady state operation the test takes place at half the desired application clock frequency C_{Appclk}. The desired frequency command is indicated by the digital inputs FREQ;

(2) level shifters that convert the test signal voltages taken from various cells across the delay line to fixed voltage levels compatible with the flip-flops that sample these signals every rising edge of C_{Sample};

(3) a charge pump that takes as input an even number of digital inputs (taps) and produces an analog reference voltage V_{Ref};

(4) an on-chip or off-chip linear or switching voltage regulator that takes as input either the analog voltage V_{Ref} or the digital tap outputs, producing the adaptive voltage $V_{AVS} < V_{DD}$. The AVS scheme described in this paper uses a charge pump to generate V_{Ref} and a linear voltage regulator;

(5) a clock generation logic needed to generate the AVS controller clock to the delay line C_{Avsclk} and the application clock C_{Appclk} such that proper operation of the application during transients is ensured. The AVS controller clock C_{Avsclk} is used to generate the test clock to the delay-line C_{Test}, the sampling clock to the flip-flops C_{Sample} and the precharge signal to the level shifters C_{Prec}.

2.1 Resettable Delay Line Description

The delay-line in the AVS controller is made up of several identical cells as shown in Fig. 2. The cells are grouped in two overlapping sections. The first section consists of N cells that model half the critical path delay of the application (referred to as the critical path model) plus a small safety margin. The next section consists of $2K$ cells whose outputs are level shifted and sampled every C_{Test} cycle.

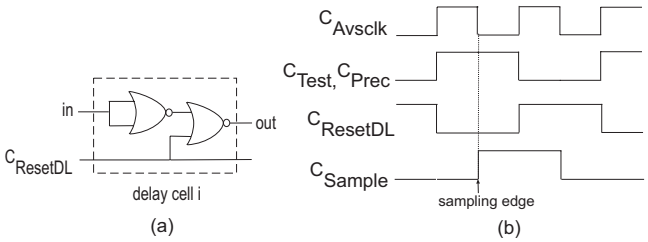

Figure 3: (a) Gate-level schematic of the delay-cell used in the delay-line and (b) the relation of the AVS controller clock C_{Avsclk} to the delay line test clock C_{Test}, precharge signals C_{Prec} and sampling clock C_{Sample}.

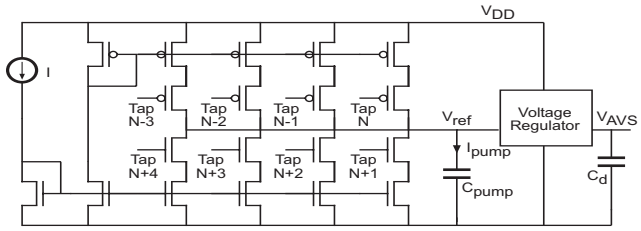

Figure 4: Charge pump for 8 delay-line taps (K = 4).

Operation of the delay-line is understood by referring to the gate level schematic of the delay-cell shown in Fig 3(a) and the idealized clock waveforms of Fig. 3(b). When the test clock C_{Test} is low, all delay-cell outputs are reset to logic 0. When C_{Test} is at logic 1, the test signal propagates from in to out via the logic gates. For the first delay-cell, in is connected to C_{Test}. At the end of the test, the output TAPi is set to logic 1 if the supply voltage V_{AVS} is sufficient for the test signal to propagate through the respective delay cells. The resettable delay line makes it possible to repeat the delay test in every test clock cycle at a frequency $f_{Test} = f_{Avsclk/2}$.

2.1.1 Modeling the critical path

It has been shown that the delay of a simple logic gate can be used to accurately represent the delay in more complicated structures based on standard-cell logic [9, 10]. For a given process/temperature corner, suppose that the application is designed to operate at the maximum supply voltage, and the maximum clock frequency $f_{Appclk,max}$. Using the model parameters for that process corner, the delay-line length N is selected such that the test clock C_{Test} is just able to propagate through this length when the supply voltage to the delay-line has the maximum value, but not able to propagate through delay-cell $N+1$. An even number of delay-line taps are then taken around the tap that corresponds to the delay-cell N.

Since the test takes one half of the AVS controller clock period (i.e. when C_{Avsclk} is at logic 1), the critical path model effectively captures half of the application critical path delay.

2.2 Charge Pump and Voltage Regulator

Fig. 4 illustrates the charge pump for a delay-line with $2K$=8 taps. It is assumed that the taps are taken from consecutive delay cells. In steady state, the taps $N-3$ through N are at logic 1 (i.e. V_{AVS} is sufficient for the test clock to propagate through), while the taps $N+1$ through $N+4$ are at logic 0. As a result, all pump

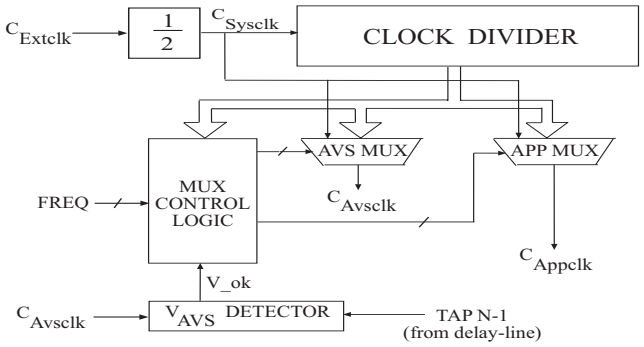

Figure 5: Block diagram schematic of the proposed clock generation scheme for generation and updates of C_{Avsclk} and C_{Appclk}.

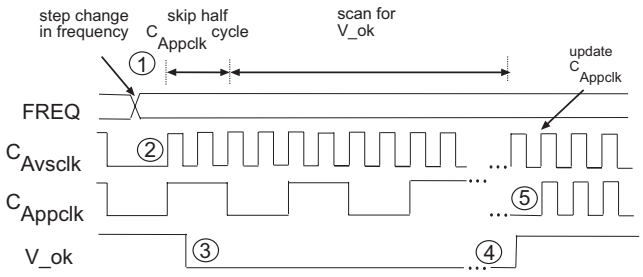

Figure 6: Timing diagram showing the process of updating C_{Avsclk} and C_{Appclk} for a step increase in frequency.

devices are off. If, for example, the supply voltage is higher than necessary, one or more NMOS pump devices is turned on, thus discharging the C_{pump} capacitor. The use of multiple taps extends the range across which the pump output current is proportional to the error in voltage, thus improving the large-signal transient response. The reference voltage V_{Ref} is buffered by a voltage regulator to produce the supply voltage V_{AVS}. The voltage regulator can be a high-efficiency switching regulator to maximize the power savings, or a linear regulator. The advantages offered by the use of a linear regulator are (a) it can be integrated on-chip; (b) V_{AVS} is not affected by switching noise; and (c) the transient response is fast.

2.3 Clock generator

A basic requirement for AVS implementation is that the application operates properly over frequency step changes which result in changes to V_{AVS}. This is automatically satisfied in AVS controllers where the system clock is generated by a VCO controlled by the supply voltage [2, 10, 12]. However, in this approach, noise in the supply voltage V_{AVS} may result in increased system clock jitter. In our implementation, shown in the block diagram of Fig. 5, a clean low-jitter external clock C_{Extclk} is generated separately, and additional control logic is used to correctly update the application clock through the transients.

The clock C_{Sysclk} is input to a synchronous divide-by-256 counter with outputs taken of every divide-by-2 stage. In general, any other frequency scaling of C_{Sysclk} is permissible. The outputs of this counter and C_{Sysclk} are then selected to be the AVS controller clock C_{Avsclk} and the application clock C_{Appclk}. The selection control logic works as follows : given the desired frequency indicated by the FREQ control bits, the update of the clocks C_{Avsclk} and C_{Appclk} takes place at the C_{Sysclk} edge when C_{Sysclk} and the current and desired counter outputs go through the same logic level transition. Updating C_{Avsclk} and C_{Appclk} at this synchronization point ensures a 50% duty cycle on the clocks through any frequency change.

The indication that the supply voltage has reached the correct steady-state value is provided by the V_{AVS} digital detector. The input to this detector is TAP N-1 (cf. Section 2.1). If TAP N-1 is at logic 1 for a consecutive sequence of C_{Avsclk} cycles, the desired steady state V_{AVS} has been reached and the output V_ok is set to logic 1.

2.3.1 C_{Avsclk} and C_{Appclk} Mux control logic

Operation of the mux control block is illustrated by the timing diagram in Fig. 6. It is assumed that the AVS control loop is operating at some steady state operating point before a step change in frequency is registered at the inputs to the control block.

(a) *C_{Avsclk} and C_{Appclk} behavior for increase in speed*

If there is a desired increase in frequency the V_{AVS} needs to reach the appropriate increased steady state value before C_{Appclk} can be updated. With reference to Fig. 6 the control logic works as follows :

(1) When the step increase in frequency occurs, the desired frequency is locked from any further changes until all updates are completed.

(2) At the next synchronization edge C_{Avsclk} is updated to the desired frequency. This decreases the test clock period and results in more TAP outputs going to logic 0, causing V_{AVS} to increase;

(3) The increased test clock frequency also results in the V_{AVS} detector pulling the V_ok signal to logic 0. A half C_{Appclk} cycle is allowed to pass ensuring V_ok is at logic 0 and the loop transient is underway;

(4) The control logic waits for the V_ok signal to go to logic 1, indicating that the new steady state V_{AVS} voltage value has been reached;

(5) At the next synchronization edge the application clock C_{Appclk} is updated to C_{Avsclk}, and the transient process is complete.

(b) *C_{Avsclk} and C_{Appclk} behavior for decrease in speed*

If there is a desired decrease in frequency, both C_{Avsclk} and C_{Appclk} can be updated at the next synchronization edge.

3. EXPERIMENTAL RESULTS

The entire scheme described in Section 2 was designed in a 0.5 μ standard CMOS process. The area taken by the AVS controller excluding pads is 0.12 mm^2. The chip also contains two 16x16 array multiply and accumulate (MAC) blocks. Input to a MAC is provided by a 32-bit maximal sequence linear feedback shift register (LFSR) that provides a pseudo random input sequence. The dual-MAC and LFSR form the application block. For easy verification of the application, a third MAC and LFSR operates at constant V_{DD}. Its outputs are compared with the level-shifted application block outputs operating at V_{AVS} every application clock cycle.

The application block was designed around a typical process corner to operate at a maximum application clock frequency of 20 MHz and a maximum supply voltage of 2.4 V. A model extracted from layout of the delay-line was simulated for the typical process corner at 20 MHz and 2.4 V to determine the delay-line length N of 36 delay cells (cf. Section 2.1.1). Referring to Fig. 2, eight delay-line taps were taken from alternate delay cells between delay cells 30 (tap 0) and 36 (tap 3), and between delay cells 37 (tap 4) and 43 (tap 7). Delay cell 34 (tap 2) was used as the input to the V_{AVS}

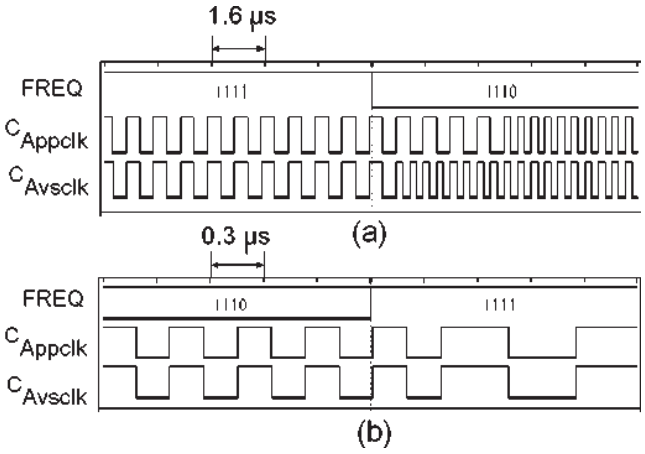

Figure 7: Experimental waveforms of C_{Avsclk} and C_{Appclk} illustrating the proposed clock generation and update scheme. The two application clock frequencies are $f_{1,Appclk}$ = 1.25 MHz and $f_{2,Appclk}$ = 2.5 MHz.

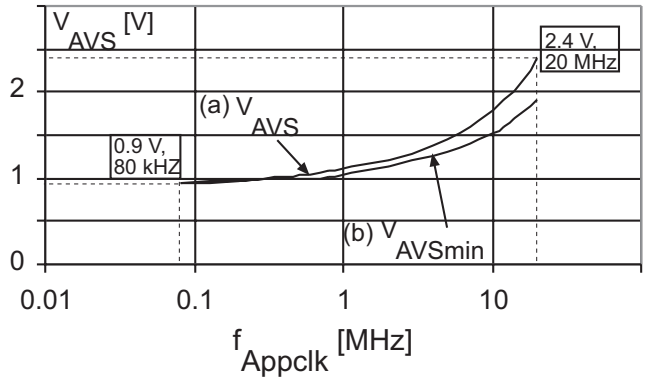

Figure 8: Experimental plot of (a) V_{AVS} as a function of f_{Appclk} for a closed loop AVS test and (b) V_{AVSmin} as a function of f_{Appclk}, where V_{AVSmin} is the minimum voltage at which the application operates correctly.

detector.

Operation of the AVS controller clock C_{Avsclk} and the application clock C_{Appclk} at the frequency step change boundary is illustrated by Fig. 7. For clarity, the step change is shown for a 2X change in speed between $f_{1,Appclk}$ = 1.25 MHz and $f_{2,Appclk}$ = 2.5 MHz. As described in Section. 2.3.1: in Fig. 7(a) C_{Avsclk} changes to the higher frequency and once V_{AVS} is at the new steady state value, C_{Appclk} is updated to the desired frequency. In Fig. 7(b) for a 2X decrease in speed, both clocks are updated at the next synchronization edge.

Fig. 8 shows the desirable operation of the closed-loop supply voltage V_{AVS} tracking V_{AVSmin} with a small safety margin. The voltage V_{AVSmin} (curve (b)), which is the minimum voltage at which the application operates correctly, is determined in an open-loop test. The plot shows closed loop operation for a wide frequency range from 80 kHz (V_{AVS} = 0.94 V) to 20 MHz (V_{AVS} = 2.38 V).

Fig. 9 shows the measured power consumption of the application as a function of f_{Appclk} relative to the power consumed at constant

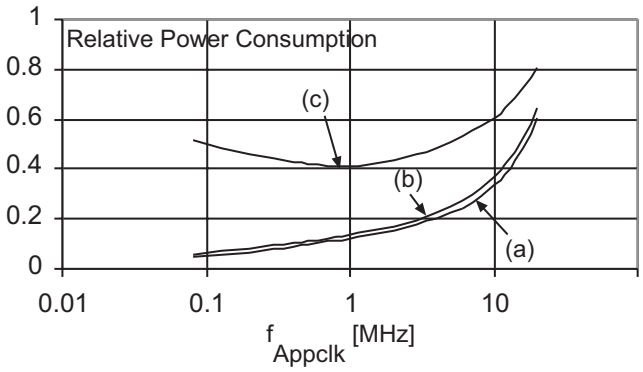

Figure 9: Comparison of the measured power consumption relative to the power consumed at constant V_{DD} = 3 V : (a) for AVS, application only; (b) for AVS, application and controller; and (c) for AVS, application, controller and linear voltage regulator.

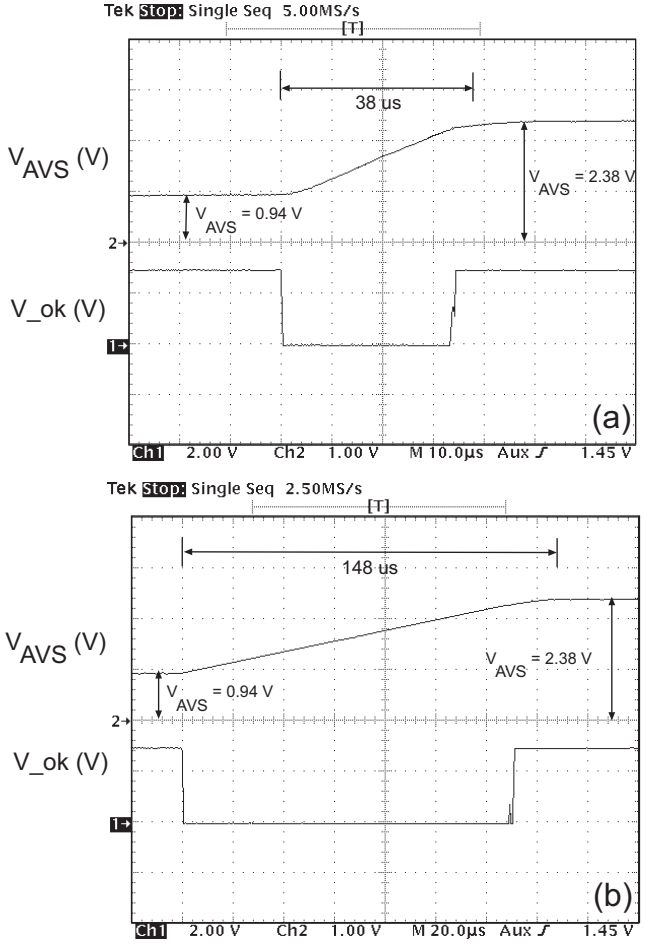

Figure 10: Details of experimental AVS closed loop transient response for a step increase in speed from $f_{1,Appclk}$ = 80 kHz to $f_{2,Appclk}$ = 20 MHz for (a) all 8 taps as inputs to the charge pump, and (b) only 2 taps (taps 3 and 4) as inputs to the charge pump.

V_{DD} = 3 V. With a linear regulator (curve (c)), the power savings are reduced compared to an ideal 100% efficient regulator (curve (b)). The plot also points to the importance of power efficiency of the voltage regulator, especially at very low throughput. For reference, the power consumed at V_{DD} = 3 V and f_{Appclk} = 20 MHz is 40 mW. The AVS controller losses scale with the application power. At 20 MHz the controller power consumption is 2 mW, an advantage of the simple implementation of the proposed scheme.

Fig. 10 shows the details of the transient response in the vicinity of the step change when (a) all 8 taps are used and (b) when only two taps were used. When all 8 taps are used, the transient between V_{AVS} = 0.94 V (f_{Appclk} = 80 kHz) and V_{AVS} = 2.4 V (f_{Appclk} = 20 MHz) takes about 38 μs which compares favorably to results reported in earlier publications [3, 5, 7, 10, 12].

4. CONCLUSIONS

Adaptive voltage scaling (AVS) of a supply voltage is emerging as an effective power management technique for digital VLSI applications. The paper describes a delay-line based regulation scheme targeted towards standard-cell ASICs. The proposed scheme is simple to implement, allows fast transient response to step changes in speed, and stable operation over a very wide range of frequencies. The delay is measured at half the system clock rate which minimizes the system latency. The small complexity of the controller implies that it takes an area of 0.12 mm^2 and a power consumption of 2 mW at 20 MHz. A linear regulator was used as the power supply and has the advantage of an on-chip implementation of the proposed AVS scheme. A chip including the AVS controller and a dual 16-bit MAC has been fabricated in a standard CMOS process. Experimental results demonstrate closed loop operation over the frequency range from 80kHz to 20MHz, and a 38 μs transient response for a step change in the application clock frequency from 80 kHz to 20 MHz.

5. ACKNOWLEDGMENTS

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