

An Efficient Model for Frequency-Dependent On-Chip Inductance

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Abstract

In this paper, we propose an efficient table-based model for frequency-dependent on-chip inductance, and apply it to compute mutual inductance between random wires and loop inductance for cascade wires, respectively. Our inductance computation achieves around 5% error when compared to the numerical solution, and matches frequency-dependent impact very well. We also apply the inductance model to generate RLC circuit models for on-chip interconnects, and present a complexity-efficient normalized RLC circuit model for multiple parallel wires. These results are extremely efficient, and can be effectively used during iterative design procedure. Further, the table-based inductance model has been implemented as a Web-based tool to generate inductance matrix for given random wires.

1. INTRODUCTION

The inductance for on-chip interconnects shows growing importance as we move towards multi-gigahertz designs [14, 3, 9]. In order to better simulate and optimize on-chip interconnects, the inductance of on-chip interconnects need to be extracted from the interconnect geometry. This extraction must be accurate as a correlation with “final” verification engines, and is needed for design convergence. The extraction must also be efficient, because it may be performed dozens of times on the full-chip level and thousands of times on critical nets. Clearly, numerical extraction [16, 10, 17] is hard to support during iterative procedures of simulation and optimization. In [7], an efficient table-based inductance model was proposed using the *partial element equivalent circuit (PEEC)* model for coplanar parallel bus structures. The method is able to consider the impact of frequency, and has been used in the state-of-the-art processor design. Later on, more general interconnect structures were considered in [15, 5], using formulae under the PEEC model. However, methods in [15, 5] are not able to consider the impact of frequency.

In this paper, we study RLC modeling for on-chip general interconnect structures (herein referred to as random wires). Our primary contribution is an efficient table-based model for frequency-dependent inductance. It is applicable to random wires, and has around 5% error when compared to the numerical solver. We

also apply this model to compute the loop inductance and to generate RLC circuit models for random nets, and achieve satisfied results in an efficient way.

In the rest of the paper, we present our inductance model and compare it to the numerical solver in Section 2, and apply the model to generate RLC circuit models for random wires in Section 3. Particularly, a complexity-reduced RLC circuit model is described in Section 3. We conclude in Section 4.

2. INDUCTANCE MODEL

In this section, we first present the inductance extraction solution to the twin coplanar wires, then solve random wires in multiple layers based on the solution for the twin coplanar wires. We finally compare our approach with the numerical field solver.

2.1 Twin coplanar wires and random wires

The twin coplanar wires are special cases of the aligned coplanar wires. If multiple parallel wires are located in the same layer, all have the same length and thickness, and all starting (as well as ending) points are aligned, we call these wires *aligned coplanar wires*. An example of two aligned coplanar wires is given in Figure 1. When the two wires have the same width, we call them *twin coplanar wires*.

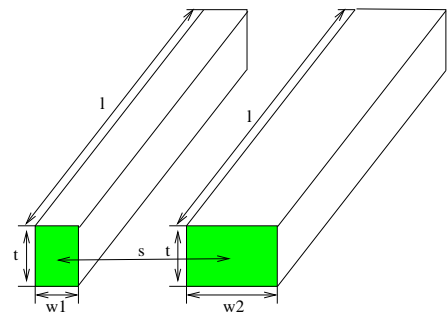


Figure 1: An example of two aligned coplanar wires. The two wires are located in the same layer and are aligned. They have the same length l , same thickness t , but different widths w_1 and w_2 . The center-to-center space between them is s .

We call any parallel wires as *random wires*. Differing from aligned coplanar wires, random wires may be located in different layers, have different widths, lengths and thicknesses. An example of two random wires is shown in Figure 2. In addition to widths w_1 and w_2 , thicknesses t_1 and t_2 , and lengths

l_1 and l_2 , the two random wires are characterized also by the horizontal space s , the vertical space v , and the displacement of the starting ends d . Obviously, the twin coplanar wires is a special case of two random wires. Note that both aligned coplanar wires and random wires are defined for parallel wires. The definitions will be justified in Section 2.3.

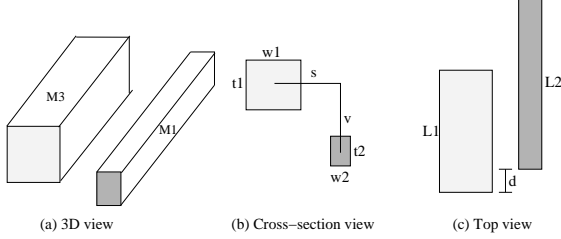


Figure 2: An example of two random wires in different layers (layer M3 and layer M1): (a) 3D view, (b) Cross-section view, and (c) Top view. The two wires have lengths (l_1, l_2) , widths (w_1, w_2) , thicknesses (t_1, t_2) , as well as horizontal and vertical spaces (s, v) . The displacement of the starting ends of the two wires is d .

2.2 Inductance model for twin coplanar wires

Based on the PEEC (partial element equivalent circuit) model [17], the following Observations were made in [7]:

OBSERVATION 1. *Self partial inductance of a wire is solely decided by the wire itself.*

OBSERVATION 2. *Mutual partial inductance between two wires is solely decided by the two wires themselves.*

A table based method can be developed for the twin coplanar wires using Observations 1 and 2. The self inductance can be pre-computed and stored in a four-dimensional table, and mutual inductance in a five-dimensional table. Specifically, the self inductance L_s can be represented by

$$L_s = L_s(l, w, t, f), \quad (1)$$

and the mutual inductance L_m^t for the twin coplanar wires can be represented by

$$L_m^t = L_m^t(l, w, t, s, f), \quad (2)$$

where l, w, t are the length, width and thickness of the twin coplanar wires, respectively, s is the space between the twin coplanar wires, and f is the extraction frequency.¹

2.3 Inductance model for random wires

Solving inductance extraction for random wires will lead to the inductance extraction solution for all wires at the full chip level. Observations 1 and 2 were proved without using the assumption of aligned coplanar wires [7]. Therefore Observations 1 and 2 still hold for random wires, and the self inductance for any wire

¹The frequency for inductance computation is not clock frequency, but is decided by the signal rising time t_r . The knee frequency can be defined as $F_{knee} = 0.5/t_r$ and be used as the frequency to compute inductance, as “the behavior of a circuit at frequencies above F_{knee} hardly affects digital performance” [8]. A similar conclusion was drawn in [12] using the concept of “significant frequency”.

can still be pre-computed and stored in a four-dimensional table $L_s(l, w, t, f)$.

In addition to Observations 1 and 2, there is another well-accepted Observation:

OBSERVATION 3. *The mutual inductance between any two orthogonal wires is negligible.*

Therefore, the mutual inductance extraction problems for the full chip can be reduced to two separated subproblems, one is to solve the mutual inductance for random wires parallel to x-axis, and the other is to solve the mutual inductance for random wires parallel to y-axis. Observations 2 and 3 justify why we define both aligned coplanar wires and random wires only for parallel wires.

If we simply use Observation 2, the mutual inductance between two random wires need to be pre-computed and stored in a ten-dimensional table $L_m^r(l_1, l_2, w_1, w_2, t_1, t_2, s, v, d, f)$, where variables from l_1 to d are defined in Figure 2, and f is the extraction frequency. To avoid building and looking-up such a huge table, we propose that the mutual inductance L_m^r between two random wires can be computed as:

$$L_m^r = \frac{L_1 + L_2 - L_3 - L_4}{2} \quad (3)$$

where

$$\begin{aligned} L_1 &= \frac{L_m^t(l_1 + l_2 - \sigma, w_1, t_1, \sqrt{s^2 + v^2})}{2} \\ &+ \frac{L_m^t(l_1 + l_2 - \sigma, w_2, t_2, \sqrt{s^2 + v^2})}{2} \\ L_2 &= \frac{L_m^t(\sigma, w_1, t_1, \sqrt{s^2 + v^2})}{2} \\ &+ \frac{L_m^t(\sigma, w_2, t_2, \sqrt{s^2 + v^2})}{2} \\ L_3 &= \frac{L_m^t(l_1 - \sigma, w_1, t_1, \sqrt{s^2 + v^2})}{2} \\ &+ \frac{L_m^t(l_1 - \sigma, w_2, t_2, \sqrt{s^2 + v^2})}{2} \\ L_4 &= \frac{L_m^t(l_2 - \sigma, w_1, t_1, \sqrt{s^2 + v^2})}{2} \\ &+ \frac{L_m^t(l_2 - \sigma, w_2, t_2, \sqrt{s^2 + v^2})}{2} \end{aligned}$$

and

$$\sigma = \begin{cases} (l_1 - d) & l_1 \leq d + l_2 \\ l_2 & l_1 > d + l_2 \end{cases}$$

Note that L_1, L_2, L_3 and L_4 are calculated by equation (2) that can be either a formula or a table as in this paper.

In order to catch the frequency-dependence, a wire is often divided into filaments (see Figure 3), where the current is assumed to be uniform within filaments. In [6], analytical formulae were given for inductance between filaments. For two non-overlap filaments shown in figure 4, equation (4) was proposed:

$$2M = (M_{l+m+\sigma} + M_\sigma) - (M_{l+\sigma} + M_{m+\sigma}) \quad (4)$$

and (5) was proposed for partial-overlap² filaments:

$$2M = (M_{l+m-\sigma} + M_\sigma) - (M_{l-\sigma} + M_{m-\sigma}) \quad (5)$$

²Partial-overlap is contrast to the total-overlap. For partial-overlap, σ is defined as the overlapped length.

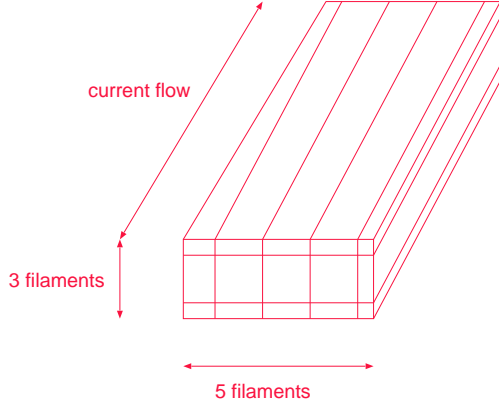


Figure 3: A wire is divided into 3×5 filaments.

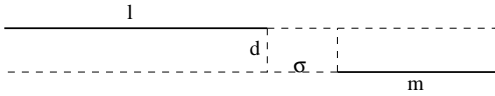


Figure 4: Two non-overlap filaments.

where M is the mutual inductance and $M_{l+m+\sigma}$, M_{σ} , $M_{l+\sigma}$, $M_{m+\sigma}$ are mutual inductance between two equal and parallel filaments with the length of the subscript.

Equation (3) extends (4) and (5) from a pair of filaments to a pair of random wires that may have different widths and thicknesses, and is able to consider non-overlap, partial-overlap and total-overlap³ cases. The frequency dependency of current distribution among filaments within a wire is caught during table building via numerical inductance computation. Note that in [7], a proof was given for Observations 1 and 2, based on the relationship between inductance for filaments and that for wires. A similar scheme can be used to illustrate the rational behind Equation (3) in this paper.

In the next subsection, we will compare the inductance values given by equation (3) with those obtained by the numerical field solver FastHenry [10].

2.4 Experimental results

We have implemented the above table-based model for frequency-dependent inductance, and proceed to compare the inductance given our model with the numerical solution by FastHenry. We consider first the mutual inductance between two random wires, and then the loop inductance of a cascade interconnect structure.

2.4.1 Mutual inductance

In our experiment, we first build a mutual inductance table by using FastHenry and the following parameters:

1. Wire length: from $0.1\mu m$ to $10000\mu m$, with 60 data points.
2. Wire width: from $0.5\mu m$ to $50\mu m$, with 10 data points.
3. Wire spacing: from $0\mu m$ to $50\mu m$, with 10 data points.
4. Frequency: from 1GHz to 100GHz, with 4 data points.
5. All data points are uniformly distributed.

³Total-overlap means one of the wire is totally overlapped with another.

We then choose 400 random cases for two random wires based on the following ranges of parameters:

$$\begin{aligned} 100\mu m < l_1, l_2 < 5000\mu m \\ 0\mu m < d < 5000\mu m \\ 0.5\mu m < w_1, w_2, t_1, t_2 < 50\mu m \\ 0\mu m < s, v < 50\mu m \end{aligned}$$

We finally solve each random case by FastHenry and table lookup using equation (3), respectively, and present all inductance values in Figure 5. As one can see that the formula approximates the mutual inductance of two random wires very well. We also give the error distribution in Figure 6. Most results of the 400 random cases have error within $\pm 5\%$. Those rare cases with error as large as 20% only occur when the inductances are fairly small and therefore can be ignored as pointed out in [3].

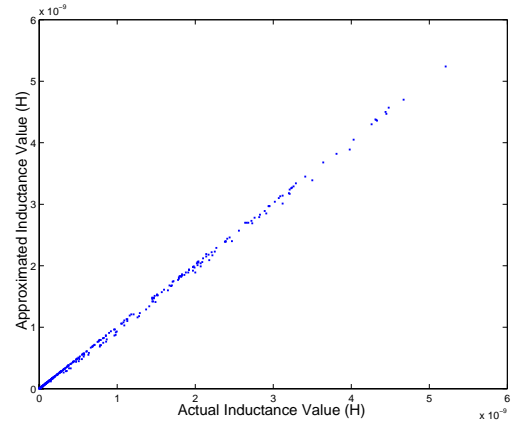


Figure 5: Mutual inductances of random wires. The x-axis is mutual inductance computed by FastHenry, and the y-axis is mutual inductance computed by table lookup and equation (3).

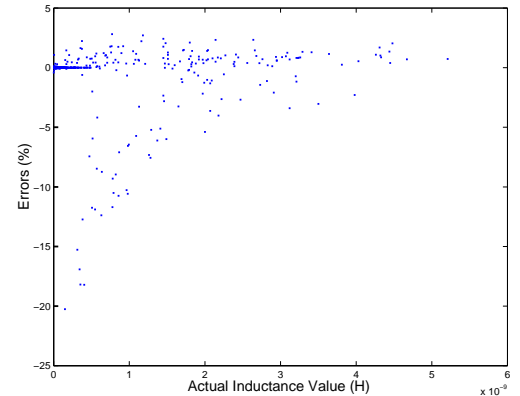


Figure 6: Error distribution of the approximated inductance. Most of the points are lie in $\pm 5\%$ error range. Larger error tends to happen when mutual inductance is relatively small.

2.4.2 Loop inductance

Our inductance model can also be used to compute loop inductance for cascade interconnect structures such as that in Figure 7. The loop inductance without consideration of mutual inductance between different wire segments is

$$L_{loop} = L_{ed} + L_{dc} + L_{cb} + L_{ba}; \quad (6)$$

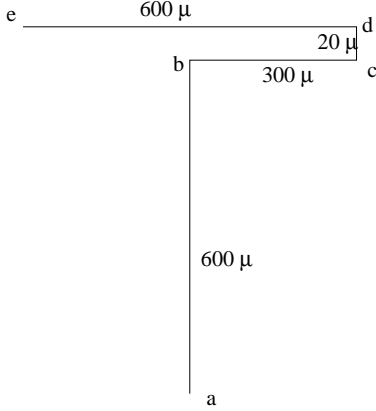


Figure 7: A cascade interconnect structure, with length shown for each segment.

where L_{ed}, L_{dc}, L_{cb} and L_{ba} are self inductance for segments ed, dc, cb and ba . It was shown in [1] that (6) leads to satisfied loop inductance value when there are coplanar shields. However, in general, the loop inductance should be computed with consideration of mutual inductance between different wire segments as

$$L_{loop} = L_{ed} + L_{dc} + L_{cb} + L_{ba} - 2 \cdot L_{ed,cb} + 2 \cdot L_{dc,ba}(7)$$

where $L_{ed,cb}$ and $L_{dc,ba}$ are mutual inductance between wire segments ed and cb , and dc and ba , respectively.

In Table 1, we compute loop inductance using the above two formulae based on self and mutual inductance given by our model, and compare it with inductance given by FastHenry. We consider frequencies from $100MHz$ to $100GHz$, and consider wire width of $1.2\mu m$ and $12\mu m$, respectively. The wire thickness is $1.0\mu m$ and $2.0\mu m$, respectively. As shown in this table, compared to FastHenry, the loop inductance without consideration of mutual inductance has error from 23.5% to 37.2%, and the loop inductance considering mutual inductance has an error less than 5%. Further, the loop inductance considering mutual inductance based on our inductance model catches the frequency variation very well. The frequency variation is 2.1% for $1.2\mu m$ wire width, and is 6.4% for $12\mu m$ wire width.

3. RLC CIRCUIT MODELS

In this section, we present two RLC circuit models: the *full model* and the *normalized model*. In general, the full model is applicable to random wires, whereas the normalized model is applicable only to aligned coplanar wires. Because the normalized model has a much reduced complexity, but achieves waveforms comparable to those given by the full model, the normalized model is a natural choice for aligned coplanar wires when compared to the full model and model order reduction techniques such as [13, 4].

3.1 Full and normalized models

For the simplicity of presentation, we consider in this section that there are m aligned coplanar wires (or simply, *wires*), each uniformly divided into n segments. The two circuit models have identical elements for resistance and capacitance. Each wire segment has a resistance given by a simple formula, and has ground capacitance and floating coupling capacitance connected to adjacent wire segments. All capacitance values are computed by using the $2\frac{1}{2}D$ capacitance extraction method [2].

The two circuit models have different inductance elements. In the full model, a self inductance element is built for every wire

segment, and a mutual inductance element is built for every pair of wire segments. Both values are computed according to the approach presented in Section 2. For m wires, each with n segments, the full model has $m \times n$ elements for self inductance, and $C_{m \times n}^2$ elements for mutual inductance as there is mutual inductance between any two wire segments, no matter the two segments belong to the same wire, or different wires.

Figure 8(I) shows a full RLC model for the twin coplanar wires that have two segments each wire. We label the two wires as wire a and wire b , and there are four segments $a1, a2, b1$ and $b2$. The full RLC circuit totally has $2 \times 2 = 4$ self inductors, and $C_4^2 = 6$ mutual inductors. Given length l , width w , thickness t and spacing s , the self inductance values of L_{a1}, L_{a2}, L_{b1} and L_{b2} are computed by $L_s(l/2, w, t, f)$ under frequency f . Mutual inductance is represented by inductive coupling $k_1 \sim k_6$, as an example, inductive coupling k_1 is given by $k_1 = \frac{L_{m-a1,b1}}{\sqrt{L_{a1} \times L_{b1}}}$, where L_{a1} and L_{b1} are self inductance of segments $a1$ and $b1$, $L_{m-a1,b1} = L_m^t(l/2, w, t, s, f)$ is the mutual inductance between these two segments.

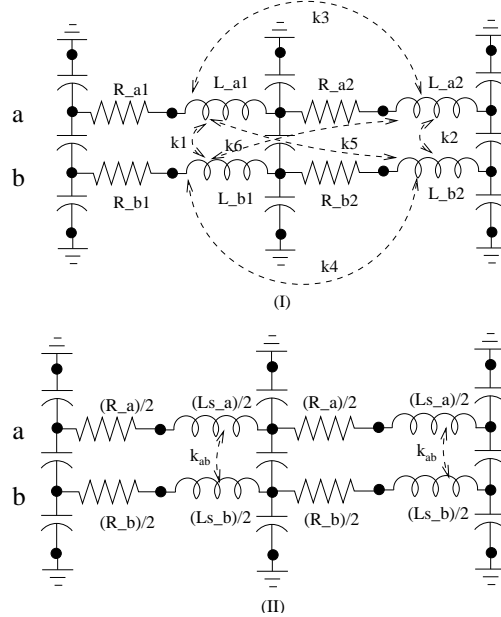


Figure 8: RLC models for two wires, each has two segments: (I) full model, and (II) normalized model.

In the normalized model, mutual inductance only exists between aligned segments. For the same twin coplanar wires (see Figure 8(II)), the normalized circuit has $2 \times 2 = 4$ self inductors, and $(2 - 1) \times 2 = 2$ mutual inductors. Let L_s be the self inductance of one wire of the twin coplanar wires, i.e., $L_s = L_s(l, w, t, f)$, each wire segment in this two-segment model has self inductance $L_s/2$. If there are n segments for a wire with self inductance L_s , then each wire segment has self inductance L_s/n . In the meantime, the inductive coupling k_{ab} between wire segments does not change with respect to the wire segmenting, and is given by $k_{ab} = \frac{L_{m-a,b}}{\sqrt{L_a \times L_b}}$, where L_a and L_b are self inductance of wires a and b , respectively, $L_{m-a,b} = L_m^t(l, w, t, s, f)$ is the mutual inductance between the two wires.

As compared with the full model, the total number of self inductors in the normalized model is still $m \times n$, where m is still the number of wires, n the number of segments. However, the total number of mutual inductors of this model is drastically

width=1.2 μ m, thickness=1 μ m				
Frequency	100M	1G	10 G	100G
FastHenry	1.569nH (0.0%)	1.569nH (0.0%)	1.567nH (0.0%)	1.536nH (0.0%)
loop inductance w/o mutual	1.938nH (23.53%)	1.938nH (23.53%)	1.936nH (23.55%)	1.905nH (24.02%)
loop inductance w mutual	1.519nH (-3.2%)	1.498nH (-4.5%)	1.580nH (0.8%)	1.501nH (-2.3%)
width=12 μ m, thickness=2 μ m				
Frequency	100M	1G	10 G	100G
FastHenry	1.078nH (0.0%)	1.070nH (0.0%)	1.034nH (0.0%)	1.013nH (0.0%)
loop inductance w/o mutual	1.451nH (34.59%)	1.443nH (34.91%)	1.410nH (36.33%)	1.390nH (37.16%)
loop inductance w mutual	1.064nH (-1.3%)	1.026nH (-4.1%)	0.999nH (-3.4%)	1.029nH (1.6%)

Table 1: Comparison between loop inductance for the cascade interconnect structure in Figure 5. Percentages of errors are computed with respect to inductance given by FastHenry.

reduced from $C_{m \times n}^2$ to $C_m^2 \times n$. So the normalized model has a much reduced complexity.

Note that the inductance is not linearly scalable. In general,

$$L_s(l/n, w, t, f) \cdot n \neq L_s(l, w, t, f)$$

$$L_m^t(l/n, w, t, s, f) \cdot n \neq L_m^t(l, w, t, s, f)$$

Therefore, the full model and normalized model will have different inductance values for the same wire segment.

3.2 Comparison between full and normalized models

We use two coupled wires in 100nm NTRS technology [18] to illustrate the difference between the full model and the normalized model. Both wires are 1000 μ m long, 3 μ m wide and 2 μ m thick. The center-to-center space between them is 6 μ m, and each wire is divided into 32 segments. The drivers are 200x of the minimum inverter, and the receivers 40x of the minimum inverter. The loading capacitance after each receiver is 0.05pf, and the input rising time for each driver is 28.6ps. We assume that both inputs switch at the same time but in opposite directions.

We employed HSPICE simulations to obtain the waveform at the far-end of the wires (the input nodes of receivers), and show far-end waveforms under both models in Figure 9. As one can see that the difference between using the full and normalized models is negligible.

We have run experiments for a large number of coupled wires for different number of wires and segments, different wire widths and spaces. All experimental results support the following observation:

OBSERVATION 4. *The difference in terms of waveform between full model and normalized model is negligible for aligned coplanar wires.*

The running time of full model circuit is significantly longer than that of normalized model circuit. Our illustration example took the full model 99.0 seconds, and took the normalized model only 9.1 seconds on the same computer. Therefore, the normalized model should be always used for aligned coplanar wires.

Note that the normalized model has been used in practice for aligned wires, but without theoretical explanation or experimental verification presented in [7]. However, it is worthwhile to point out that this model is in general *not* applicable to non-aligned wires.

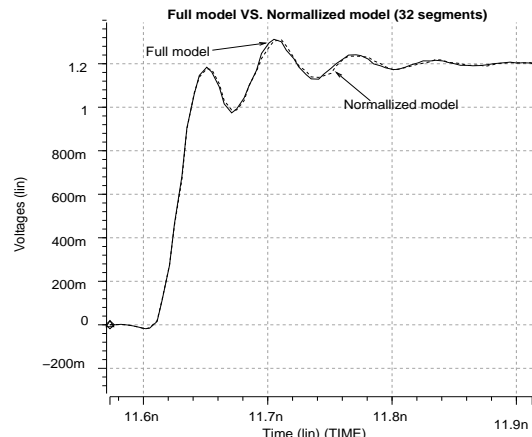


Figure 9: Far-end waveforms under the full and normalized models.

4. CONCLUSIONS

We have presented an efficient table-based model for frequency-dependent on-chip inductance, and have applied it to compute mutual inductance between random wires and loop inductance for cascade wires, respectively. Our inductance computation achieves around 5% error when compared to the numerical solution, and matches frequency-dependent impact very well. We have also applied the inductance model to generate RLC circuit models for on-chip interconnects, and have presented a complexity-efficient normalized RLC circuit model for multiple parallel wires. These results are extremely efficient, and can be effectively used during iterative design procedure. The table-based inductance model has been implemented as a Web-based tool to generate inductance matrix for given random wires. The tool can be accessed at <http://eda.ece.wisc.edu/WebHenry>. We have applied the RLC circuit models presented in this paper to several RLC interconnect analysis and synthesis works, including [19] and [11].

5. REFERENCES

- [1] N. Chang, S. Lin, L. He, O. S. Nakagawa, and W. Xie. Clocktree RLC extraction with efficient inductance modeling. In *Design Automation and Test in Europe*, March 2000.
- [2] J. Cong, L. He, A. B. Kahng, D. Noice, N. Shirali, and S. H.-C. Yen. Analysis and justification of a simple, practical 2 1/2-d capacitance extraction methodology. In *Proc. Design Automation Conf.*, pages 627–632, 1997.

- [3] A. Deutsch and et al. When are transmission-line effects important for on-chip wires. *IEEE trans on MIT*, 1997.
- [4] P. Feldman and R. W. Freund. Reduced-order modeling of large linear subcircuits via a block lanczos algorithm. In *Proc. Design Automation Conf*, 1995.
- [5] K. Gala, V. Zolotov, R. Panda, B. Young, J. Wang, and D. Blaauw. On-chip inductance modeling and analysis. In *Proc. Design Automation Conf*, pages 63–68, 2000.
- [6] F. W. Grover. *Inductance Calculations: working formulas and tables*. Dover Publications, 1946.
- [7] L. He, N. Chang, S. Lin, and O. S. Nakagawa. An efficient inductance modeling for on-chip interconnects. In *Proc. IEEE Custom Integrated Circuits Conference*, pages 457–460, May 1999.
- [8] H. Johnson and M. Graham. *High-Speed Digital Design – A Handbook of Black Magic*. Prentice Hall, 1993.
- [9] M. Kamon, S. McCormick, and K. Shepard. Interconnect parasitic extraction in the digital IC design methodology. In *Proc. Int. Conf. on Computer Aided Design*, 1999.
- [10] M. Kamon, M. Tsuk, and J. White. Fasthenry: a multipole-accelerated 3d inductance extraction program. *IEEE Trans. on MIT*, 1994.
- [11] K. M. Lepak, I. Luwandi, and L. He. Simultaneous shield insertion and net ordering for coupled RLC nets under explicit noise constraint. In *University of Wisconsin, Technical Report, ECE-00-06*, 2000.
- [12] J. Lillis, C. Cheng, S. Lin, and N. Chang. *High-performance interconnect analysis and synthesis*. John Wiley, to appear in 1999.
- [13] A. Odabasioglu, M. Celik, and L. Pileggi. PRIMA: Passive reduced-order interconnect macromodeling algorithm. *IEEE trans. on CAD*, 1998.
- [14] L. Pileggi. Coping with RC(L) interconnect design headaches. In *Proc. Int. Conf. on Computer Aided Design*, pages 246–253, Nov. 1995.
- [15] X. Qi, G. Wang, Z. Yu, and R. W. Dutton. On-chip inductance modeling and RLC extraction of VLSI interconnects for circuit simulation. In *Proc. IEEE Custom Integrated Circuits Conference*, May 2000.
- [16] A. Ruehli. Inductance calculation in a complex integrated circuit environment. *IBM Journal of Res. and Dev.*, 1972.
- [17] A. Ruehli. Equivalent circuit models for three-dimensional multiconductor systems. *IEEE Trans. on MIT*, 1974.
- [18] Semiconductor Industry Association. *International Technology Roadmap for Semiconductors*, 2000.
- [19] L. Yin and L. He. An efficient analytical model for coupled on-chip RLC interconnects. In *Proc. Asia South Pacific Design Automation Conf.*, January 2001.