System-In-Package (SIP): Challenges and Opportunities

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Abstract - In this paper, we propose the concept of System-In-Package (SIP) as a generalization of System-On-Chip (SOC). System-In-Package overcomes formidable integration barriers without compromising individual chip technologies. The goal of SIP is to match or exceed SOC performance with lower cost. SIP technology platform that provides the needed integration is described. Applications include integrating memory with logic and integrating radio frequency ICs with high-quality (high-Q) passive components. SIP technology will unleash the innovations of designers and unlock the full potential of IC technology.

I. Introduction

During the last 30 years, IC technology has been very successfully in meeting market demands by integrating more and more transistors on the chip. Over a hundred million transistors can be made on a single die. The total amount of 10^{17} transistors is being made a year today. Each new year the semiconductor industry has made almost the same amount of transistors as all of the previous years added together. The cost per transistors has dropped six orders of magnitude. The cost is the less than 10^{-5} of a cent per transistor in DRAM and 10^{-6} of a dollar in CPU today. As Arno Penzias of Lucent pointed out, the cost of a transistor is approaching "zero cost" after the invention of the transistor 50 years ago. Moore's Law will still be valid for at least two or three more generations. It is clear from the historical perspective that the electronics industry is dramatically different from any other industry. This is accomplished by the fast advances of IC technology and the innovations of the designs.

The central driver is the integration. The most of the integration activities have been in circuits that are made in the same technology. Up until now the PC is the most important market to drive the semiconductor industry. The rest of the markets have also benefited from it.

In the 21st century, the electronic market will be driven by consumers. Consumers will demand immediate entertainment, instant access of information, and communications anywhere at any time. These services and products have to be delivered in a personalized fashion and at affordable prices. The consumer market will demand multimedia, high speed self direct networks, high speed modems and portable wireless communicators etc., at affordable price. The market requires fast time to market, higher levels of integration, higher speed, and lower power consumption products. We have developed System-In-Package (SIP) technology that can complement ULSI technology to extend the level of integration and to meet the market challenges in 21st Century.

II. The Challenges

Instead of focusing on conventional packaging issues that limit the chip performance, we will address the issue of how to expand the scope of integration where single chip integration becomes either impossible or not cost effective. The IC technology may be capable to put one billion transistors on a single chip in the 21st century. Therefore, it means that any circuit will only occupy a very small Si real estate. It will make SIP easier to implement.

In the 21st century, the new challenge is not how many transistors can be built on a single chip, but rather how to integrate diverse circuits together predictably, harmoniously and cost effectively.

In the past, device integration has successfully responded to new challenges. Today's emphasis regarding system-on-chip is concerned with packing different transistor technologies for different functions onto a single chip. Designers hope to merge memory with logic, mixed-signal applications with digital, and integrated passive components with active circuits. Unfortunately, merging any of the above would compromise each of individual technologies and increase the complexity and, therefore, the cost of the manufacturing process. It would also adversely affect new product time to market. Noisy digital circuits would be difficult to integrate with noise-sensitive analog circuits. Memory cells would cost more to fabricate for embedded dynamic random access memory (DRAM) than for discrete DRAM. In some cases, integration would be simply impossible. For example, high-frequency communications require circuits with a predominant amount of high-quality (high-Q) passive components that cannot be integrated within a single chip while maintaining the highest level of performance.

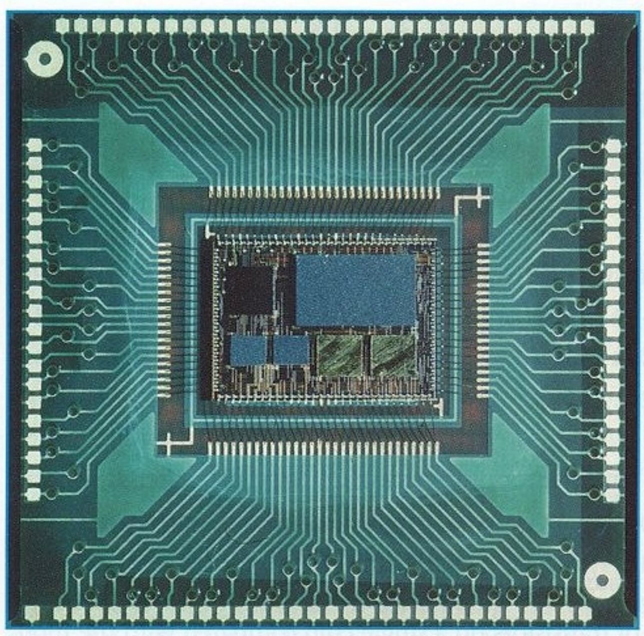

Figure 1. A system-in-a-package (SIP) for a cordless phone handset comprising six integrated circuits flip-chip attached to a silicon interconnection substrate with embedded passive components wirebonded to a laminate package.

For these reasons, a new level of integration and innovation is required to meet the circuit- and system- level challenges of the 21st century. We will present a SIP technology platform that, at its core, consists of the concept of building efficiencies by intelligently managing the system components. The goal is to match or exceed single on-chip performance with lower cost. To achieve the required level of system integration, our approach is to build the system-in-package (SIP) that overcomes formidable integration barriers without compromising individual chip technologies. The platform uses ICs designed and fabricated by their individually optimized processes. Analog and digital circuits can be brought together to function as if they were integrated but without the noise issues of a single-chip solution. Memory and logic can be integrated at lower cost and reduced size. High-frequency circuits can be integrated with high-Q passive components in an electrically friendly environment, resulting in predictable and improved performance.

III. The SIP Technology Platform

The on chip clock frequency is now in the multiple hundred MHz while the motherboard of PC can only support sub hundred MHz. The heavy off chip penalties have forced the designers to only consider single chip integration. We have identified four major areas where the new packaging technology platform can complement IC integration. It will behave like on single chip. It also will preserve the same controlled environment as on chips. We also have identified a set of packaging platforms that can provide the needed integration.

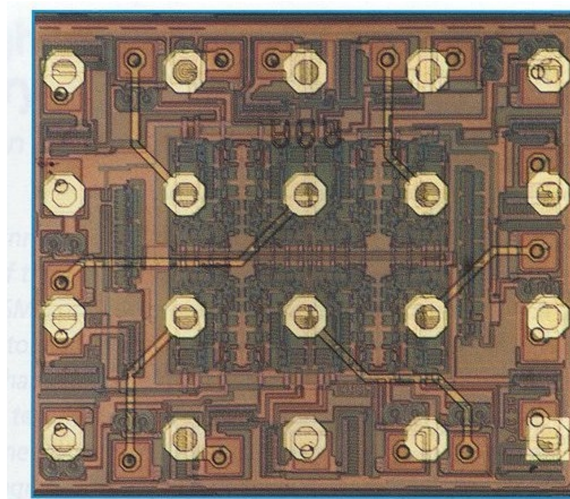

Figure 2. Perimeter wirebond pads re-routed to an area array for flip-chip assembly.

A. *Solder Bumping*

Solder bumping of ICs is essential in order to reduce package parasitics and shorten the interconnection length. The bumped ICs must have equal or better reliability and testability as in packaged ICs. The early conventional evaporated solder bumping technology by IBM has demonstrated the high reliability, but the cost of the technology may not be suitable for low cost products. The high lead solder can be easily evaporated, but lead emits alpha particles and requires high reflow temperature. It may not be suitable for laminate substrates. This is why we have developed a new bumping technology based on solder paste. When the area bump array is implemented, even stencil print & reflow solder bumps will provide sufficient bumps for most applications. Since most of the ICs have perimeter I/Os, we have developed an I/O rerouting technology to redistribute I/Os from perimeter to area array as shown in Fig. 2. When the IC designers start to design the I/O in area array format, the rerouting will not be necessary.

B. *Flip-Chip Assembly*

Flip-chip assembly either inside the packages or directly on the board is the cornerstone of the SIP. There are two basic options for flip-chip assembly. (1) Print/place/reflow: the chip

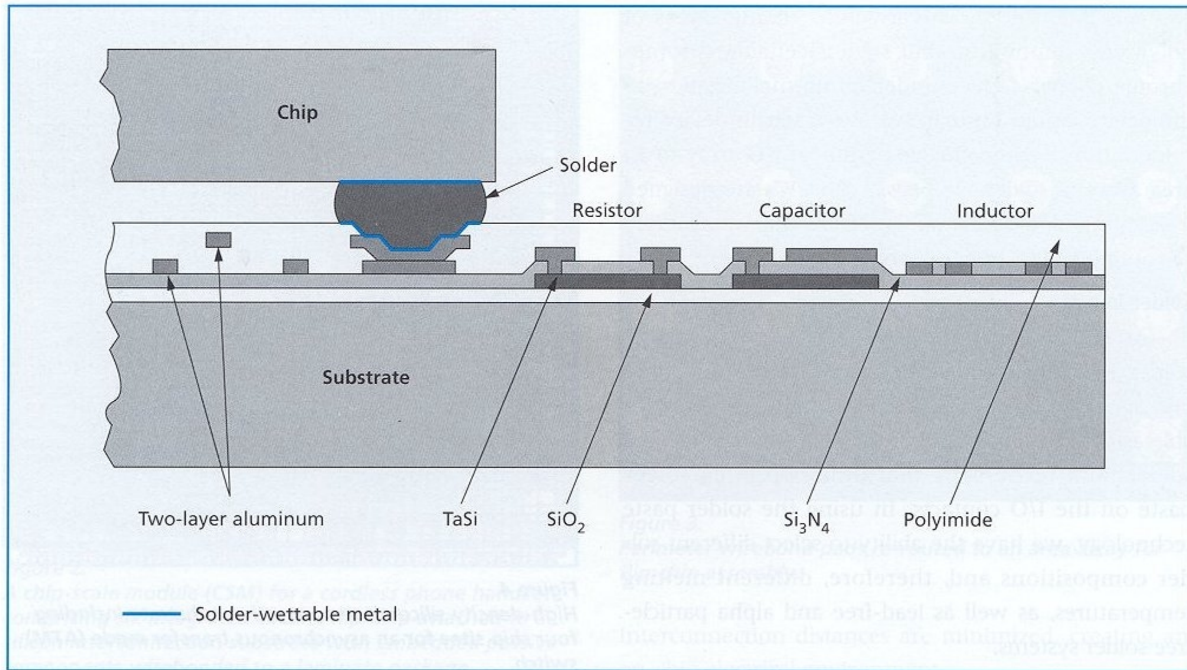

Figure 3. Cross section of an integrated circuit flip-chip assembled to a high-resistivity substrate embedded with high-Q passive components.

and substrate are either bumped or terminated with under bump metallization (UBM). The assembly process consists of printing solder paste, placing the chips, and reflowing the entire assembly to form the solder joint. (2) Bump/tack/reflow: the chip and substrate are bumped first, then chips are placed and tacked on the substrate followed by reflow. The chips can be tacked either by tacky flux or thermal compression tack. The key here is how to achieve high throughput and high yield. This is why we focused on Micro Surface Mount Technology[3]. We leverage surface mount technology to do flip-chip assembly. The bare dies are much lighter in weight than the packaged dies. Therefore the self-alignment of the solder reflow is much more effective. The Micro Surface Mount assembly throughput and yield would be better than conventional SMT.

C. *Thin Film Substrate with Integrated Passive Components*

Thin film substrate with integrated passive components is essential to support high density solder bumped ICs and minimum separation between chips. The miniaturization by integrated passive components can lead to cost reduction rather than cost increase[4-6]. The better electrical environment will also reduce the noise[7,8]. The passive components are often found in mixed signal and RF circuits. High Q inductors are essential for RF IC designs. It is difficult to integrate the high Q inductors in ICs. Today the only way to do this is to use high Q discrete inductors. The interconnection has to be low parasitics. However, the parasitics of the IC packages in between the IC and the discrete inductors will cause interference in the RF circuits. We have developed integrated high Q inductor technology that can be accurately modeled[9,10]. The integrated passive components together with flip-chip assembly and fine line interconnection will provide ultimate SIP Integration. If integrated passive components and high density interconnect are needed, then Si substrate is clearly preferred.

A typical SIP structure is shown in Fig.3. The Aluminum is the metallization for interconnection. The typical line width varies from 10 microns to 20 microns and the typical thickness is in the range of 2 to 3 microns. The interlayer dielectric is a photo definable polyimide with a typical thickness of 3 to 5 microns. The typical via size is 15 microns or larger. The Ta-Si thin film resistor is used for integrated resistors. The resistance value of the resistor is typically 500 k ohms or less. The dielectric for the capacitor is Si nitride. The resistor film may be used for the bottom electrode. One nf or less capacitors can be conveniently fabricated. As an example application shown in Fig.1, a 9mm x 6mm substrate integrated six mixed signal ICs and 200 discrete components. It uses all of the elements of the platform. The same platform is capable of building high Q inductors to a design value within 5%. This will offer the opportunity to model and build RF components such as impedance matching networks, resonators, filters and transformers for RF systems. Considering the need of SIP with integrated precision passive components, a Si substrate becomes most desirable and cost effective.

D. *Printed Circuit Board Based System-In-Package*

PWB based system level packaging technology will offer low parasitic design[11] and offer the possibility of assembly module to board directly. We believe that dispensing or printed encapsulations are more flexible and cost effective than

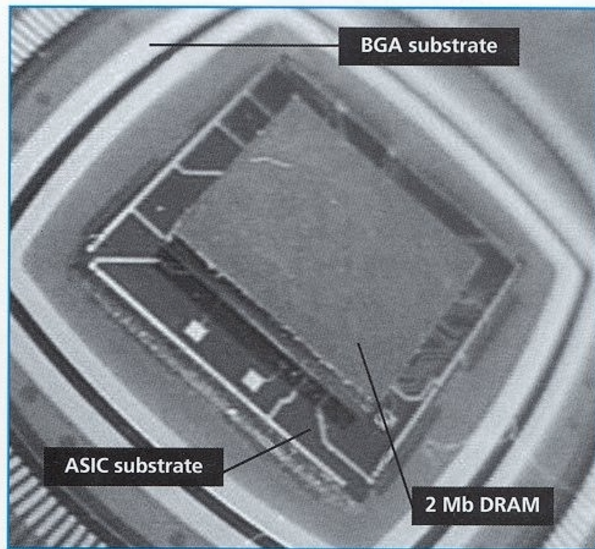

Figure 4. A dynamic random access memory (DRAM) chip flip-chip attached to an application specific integrated circuit (ASIC) chip that is wirebonded to a standard ball-grid array (BGA) package.

molding. Silicone gel and epoxy are potential candidates. The module can be either wire bonded on to the PWB or direct flip soldered onto a PWB with a hole cut in the PWB where the ICs can be inserted. In the later case, the electrical connection between the module and the components on the PWB will be very good electrically. The good electrical environment can now be further extended beyond the module. The structure of the PWB package is shown in Fig. 5. On the laminate, low I/O ICs or some discrete such as large value de-coupling capacitors may be direct flip-chip attached.

IV. The Opportunities

A. *Memory and Logic Integration*

In digital applications, single chip integration has been the only path to achieve cost reduction, integration and miniaturization. However, the strong demand for large amounts of memory needed in the systems has pushed memory and logic fabrication technologies into diverging directions. The mask levels are significantly different between memory and ASIC. The Si real estate of various memory cells built in the ASIC process is also significantly larger. There are basically three classes of chips: CPU, ASIC and memory. In memory technology development, it is important to achieve the highest possible memory density by innovations in device structures and aggressive processing technologies. In the ASIC development, it is important to achieve that the first design works. Therefore the robust and conservative design methodologies and the processing technology are important. In the CPU, the performance is most important. Therefore both design and processing have to be pushed to the leading edge.

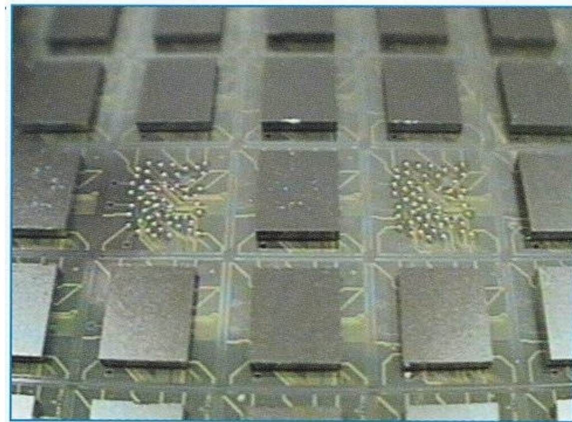

Figure 5. Dynamic random access memory (DRAM) chips flip-chip assembled on good application-specific integrated circuit (ASIC) sites with re-route interconnection visible on the ASIC wafer.

The cost per memory cell in ASIC is 20 times higher than the cost per memory cell in the standard memory chips. Therefore, there is a cost penalty to integrate a significant amount of memory in logic.

Figure 4 shows an example of SIP, which connects a bare DRAM chip onto a bare ASIC chip. First, the DRAM and ASIC chips are re-routed in wafer form. The DRAM memory wafer is then diced and placed into waffle packs or surf tape in preparation for flip-chip assembly. Lead-free solder paste is printed onto the full ASIC wafer. Memory chips are then placed onto each good ASIC device site, as shown in figure 5. After reflow to form the solder joints, the ASIC wafer is diced into individual chip-on-chip modules and readied for final packaging. The final package is physically similar to a single conventionally packaged ASIC, as shown in Figure 4.

In removing the package, performance of the DRAM memory device is shown to improve. The cumulative probability for DRAM access times has shown that essentially 100% of the functional devices exceed 26 ns at nominal supply voltage and room temperature. These devices would normally be speed-graded in conventional packages for 45 to 60 ns operation. Therefore, an opportunity exists to exploit the enhanced performance of the memory device when it is used in bare-die form. Additionally, not only did the DRAM chips perform at reduced access times, but the entire set of DRAM chips that pass the low-level functional wafer probe test also passed all the system specifications. In this case, one can envision a simplified test strategy.

B. *Radio Frequency (RF) ICs, and High-Quality (High-Q) Passive Components Integration*

Most of the RF products are built by using discrete components. The level of integration in the IC is very small. At the board level, RF interference and unpredictable parasistics in the packages present significant challenges in design. Many

design iterations are required. The "design art" is often required to achieve a successful design. This is one of the reasons why cellular products are dominated by a few major players unlike with PC's or other consumer products. There are a few major problems in making RF products. First, inductors, resonators, filters, and matching networks are expansive. They are difficult if not impossible to integrate on the chip. Second, low noise circuits are very difficult to integrate with large signal circuits. Third, the RF interference, package parasitics make the design modeling difficult.

A better approach would be to use a SIP composed of bard-die ICs on a high-resistivity interconnection substrate containing integrated thin-film passive components. This type of SIP integrates a voltage-controlled resonator (VCO) circuit, an image-rejection filter, and a Global System for Mobile Communications (GSM) transceiver IC. Integrated passive components in the substrate and a surface-mountable varactor diode make up the rejection filter and the VCO. Before the IC can be mounted to this substrate, it must have the I/O refinished and the solder joints formed for flip-chip assembly. Figure 6 is a micrograph of the 7mm x 7mm substrate with a transceiver IC a discrete varactor diode. The fully integrated substrate is then flip-chip assembled into a ball-grid array (BGA) carrier that mounts onto an existing evaluation board.

In Using a SIP for this application, we were able to maintain the on-chip electrical environment through integration of a high-frequency IC with integrated passive components. Such an environment provides a better foundation for operation in the GHz frequency range. By using semiconductor lithographic processes to create the passive components, small tolerances were achieved. Such capability obviates the need for costly trimming of conventional board-mounted components. Additionally, given the high-resistivity substrate, high-Q inductors (>60) were fabricated – an order of magnitude higher than those possible with on-chip integration. By removing package parasitics between the IC and the passive components, we reduced the amount of series inductance and simplified the design and modeling of the active RF circuit. Overall, we were able to eliminate serious VCO resonances caused by the component package leads and the printed wiring board on which the circuit was mounted.

V. Unleashing Design Innovations

Current packages and conventional interconnection often impose limits on what chip designers would like to have. IC designers often ask the following questions:

- Why I can not have more I/Os?
- Why signals have to slow down when they pass through the package?

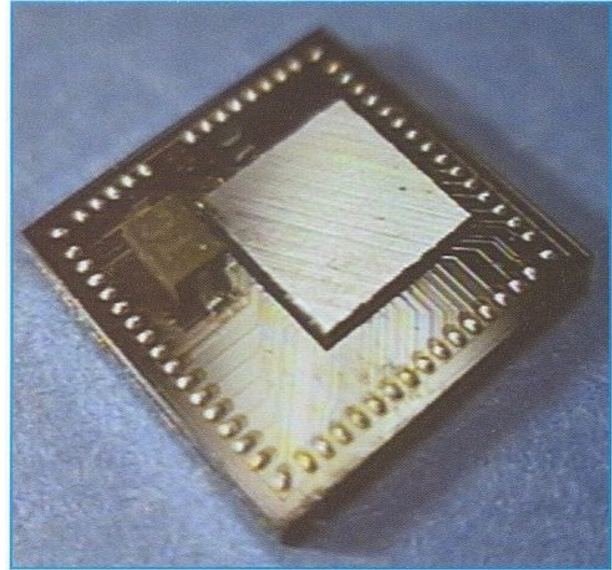

Figure 6. Global System for Mobile Communications (GSM) transceiver integrated circuit and varactor diode flip-chip attached to a high-resistivity substrate with embedded passive components solder-bumped for flip-chip placement into a ball-grid array package.

- Why it takes so much energy to communicate signals between two chips as compared to on-chip communication?

Designers often have to use costly I/O pins for the power/ground in order to maintain the signal integrity. When they run out of I/O resources, they have to MUX and DEMUX the I/Os. The SIP will address these issues simultaneously. It is possible to trade-off I/O with the speed for the same bandwidth while maintaining the signal integrity. In addition, with integrated high Q inductors and capacitors, RF IC designers can use low cost CMOS technology to design high performance RF circuits. With the new electrical environment, many new I/O design innovations can be unleashed. Since there is little or none "off-chip penalties," the innovations in architecture partitioning will be unleashed. The integration of mixed technology ICs is no longer an issue. The innovations to select an optimal chip set can be easily supported. The SIP will provide better opportunity for design reuse.

VI. Unlock VLSI Technology Potential

CMOS technology can deliver very high speed and energy efficient operations if it only has to drive a small capacitive load. If the interconnect length is short, then the interconnect line looks like a sub pf capacitor. The flip-chip eliminates the parasitic inductance of wire bonding. Thus ICs do not have to slow down at I/Os to avoid simultaneous switching noises. I/O can be located anywhere on the chip. The constraints on the I/O

count will be lifted. The bandwidth (the product of speed and the number of signal I/Os) of the ICs can be significantly increased. The signal integrity can be significantly improved [4,7]. The power consumption of inter-chip communications will be significantly reduced. With the availability of the high Q inductors and capacitors, there are will be an increase of the performances by CMOS technology for RF applications. Low noise and high Q VCO can be obtained. When CMOS can be successfully implemented in high performance RF applications, it will impact the cost of wireless products. When the difficult RF issues are removed from the PWB, it will simplify the design and manufacturing of wireless products.

VII. SUMMARY

Gordon Moor has said recently, "The electronics market is a phenomenally elastic market." It can swallow 10^{17} transistors. It is mostly swallowed by PCs. The appetite of the market will even be much larger in the 21st century. The consumer products require the power of yesterdays' super computers. Wireless communication will migrate to the global mass consumer market. Entertainment, communication and computation are merging. The phenomenal growth of the Internet is beyond everyone's expectation. Video information processing and transmission will require a much larger appetite than PC's for computing and desk top publishing.

In the 21st century, IC technology can provide "zero" cost transistors, when the designer's innovations and VLSI technology potentials are no longer blocked by packaging technology. The growth of electronics will be even higher than the past remarkable 50 years since the invention of the transistor in Bell Labs.

SIP technologies in complement to single chip integration has been developed. It has broad applications in digital, mixed signal and RF products. A global foundry infrastructure is emerging. It will have the opportunity to offer lower cost, higher performance, lower power consumption and maximum miniaturization for consumer products. Most importantly, circuit designer's innovations can be unleashed and the full potential of IC technology can be unlocked.

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