A Low Power SRAM using Auto-Backgate-Controlled MT-CMOS

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1. ABSTRACT

We have been proposed a low power SRAM using an effective method called "ABC-MT-CMOS" [1]. It controls the backgates to reduce the leakage current when the SRAM is not activated (sleep mode) while retaining the data stored in the memory cells. We also adopted a "CSB Scheme" which clamps both the source lines of the memory cell array and the bit lines. We designed and fabricated test chips containing a 32K-bit gate array SRAM. The experimental results show that the leakage current is reduced to 1/1000 in sleep mode. The active power is 0.27 mW/MHz at 1 V, which is a reduction of 1/12 of a conventional SRAM with a 3.3 V.

2. INTRODUCTION

Low power, low voltage SRAM are required for mobile systems. Although scaling of both the supply voltage and the threshold voltage of transistors enables low-power, high-speed operation, it causes a significantly increase of the static leakage current. In order to avoid this undesirable leakage current, several methods have been reported. One is called the "Variable Threshold (VT) CMOS" [2], which controls the substrate bias to reduce the leakage current in the sleep mode when the circuit does not operate. Another is called the "Multi Threshold (MT) CMOS" [3], which utilize two threshold voltages for the transistors. In this method, the higher threshold transistors cut off the leakage current in the sleep mode. The former method can retain the stored data in the sleep mode, however, it requires a triple-well structure and a charge-pump circuit. On the other hand, the latter method is simple. It, however, does lose the data stored in the memory cells, because the source line and the ground line of the internal circuit become floating nodes by high-threshold transistors. It has been reported that to avoid losing the latched data in a MT-CMOS, the stored data can take refuge in the embedded high-threshold latch circuit (balloon circuit) in the sleep mode [4]. This is not suitable for memories because of its large area overhead and design complexity. An embedded SRAM has been reported whose memory cell array blocks consist of high-threshold transistors to reduce the leakage current and whose peripheral blocks consist of low-threshold transistors to improve the access time [5]. The use of this method, however, is restricted to embedded design. It is not applicable to master-slice designs such as gate arrays.

We have adopted the Auto-Backgate-Controlled Multi-Threshold CMOS [1]. It can reduce the leakage current significantly using a simple circuit while in the sleep mode. All the transistors in the core area have a low-threshold voltage, making them suitable for master-slice chips such as gate arrays. In order to reduce undesirable leakage current in the sleep mode, the backgate bias is automatically controlled to increase the threshold voltage. Furthermore, we reduced the power when the LSI is operating by adopting the Clamped Source-line and Bit-line (CSB) scheme, which also contributes to improving the access time. We implemented the 32 K-bit SRAM using gate arrays with the above methods and evaluated the chips. In this paper, we describe the concept of the ABC-MT-

ISLPED98, Monterey, CA, USA

CMOS and its effect of reducing the power. Then we describe the CSB scheme. Finally, we report the implementation of the chip, which contains a 32 K-bit gate array SRAM, and discuss its experimental result.

3. ABC-MT-CMOS CIRCUIT

Figure 1 shows the concept of the ABC-MT-CMOS circuit. Here Q1 and Q2, which are higher threshold transistors than those for the internal circuit, act as a switch to cut off the leakage current. While the LSI is operating (which we call the "active mode"), these transistors are turned on. The virtual source line, VVDD, becomes 1.0 V supplied by the voltage source vdd1 through Q1. Another virtual source line, VGND, is forced to ground level through Q2. The internal circuits consist of only low-threshold transistors. In the active mode, the dynamic current and static leakage current flows from vdd1 to ground, as denoted by Idd (active) in Fig. 1. If the switch transistors Q1 and Q2 turn off in the sleep mode, the current Idd(active) can be reduced, however, the data stored in the memory cell disappears. In the ABC-MT-CMOS, we use the higher voltage source Vdd2 (3.3 V) and diodes D1 and D2, in order to reduce the leakage current with retaining the stored data. In the sleep mode, the VVDD is connected to Vdd2 through D1, and VGND is connected to ground through D2. Here, the diodes D1 and D2 consist of two diodes each. If we assume that the forward bias of one diode is 0.5 V, the forward voltages of D1 and D2 will be 1.0 V. Then, the VVDD and VGND become about 2.3 V and 1 V, respectively. The static leakage current Idd(sleep), which flows from Vdd2 to ground, decreases significantly compared with that of the active mode, because the threshold voltage of the internal transistors increase by its backgate bias effect. In the sleep mode, VVDD and VGND maintain their voltage levels owing to the weak leakage current Idd(sleep), so that the data stored in the memory cell is retained. This method does not require a triple-well structure and complicated circuits, such as charge pumps and balloon circuits.

Figure 2 shows the actual configuration of the ABC-MT-CMOS circuit. There are two additional high-threshold transistors Q3 and Q4. In the active mode, we apply SL = "L" and $\overline{SL}$ = "H" and Q1, Q2 and Q3 turn on and Q4 turns off. Then both VVDD and the substrate bias, BP, become 1.0 V. On the other hand, in the sleep mode, we apply SL = "H" and $\overline{SL}$ = "L" and Q1, Q2 and Q3 turn off and Q4 turns on. Then BP becomes 3.3 V. The static leakage current, which flows from Vdd2 to ground through D1 and D2, determines the voltages Vd1, Vd2 and Vm. Here Vd1 denotes the bias between the source and substrate of the p-MOS transistors, Vd2 denotes that of the n-MOS transistors, and Vm denotes the voltage between VVDD and VGND.

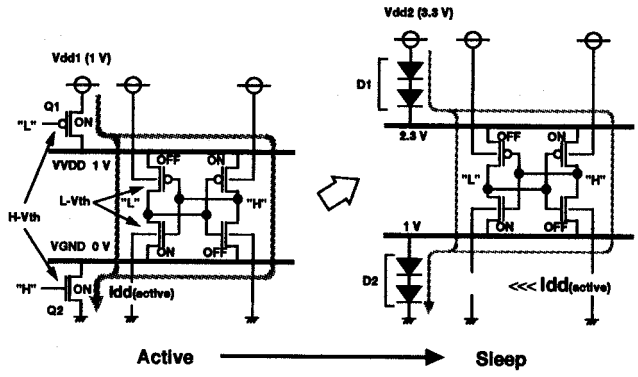

Figure 1 Concept of ABC-MT-CMOS

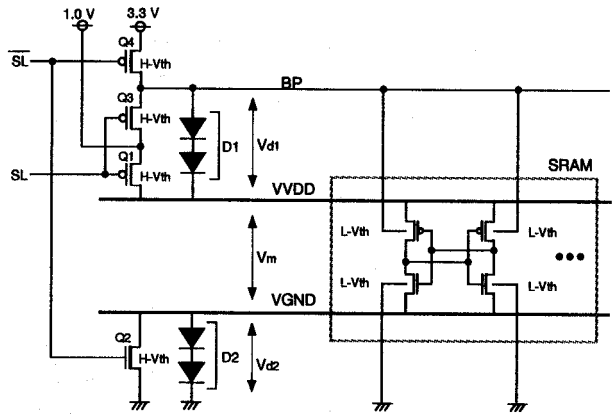

Figure 2 Configuration of ABC-MT-CMOS circuit

We simulated the static leakage current in a memory cell in the sleep mode using SPICE simulation. Figure 3 shows the leakage current per memory cell for the voltage between VVDD and VGND, denoted by Vm, which is equal to (BP - Vd1 - Vd2) as shown in Fig. 2. The horizontal axis indicates the Vm and the vertical axis indicates the leakage current on a logarithmic scale. In the graph, the solid line shows the leakage current on a memory cell circuit for the change of Vm under the BP = 3.3 V. We changed Vm by varying Vdd1 and Vdd2 simultaneously. Here, we assumed that Vd1 is equal to Vd2. It was found that the leakage current can be reduced exponentially by the reduction of Vm. When Vm = 1.0 V (Vd1 = Vd2 = 1.15 V), the leakage current is reduced to 20 pA/cell, which is comparable to a conventional memory cell which consist of high-threshold transistors and operates at 3.3 V, as shown in the figure. This means that there is a sufficient increase in the threshold voltage of the circuit due to the backgate effect.

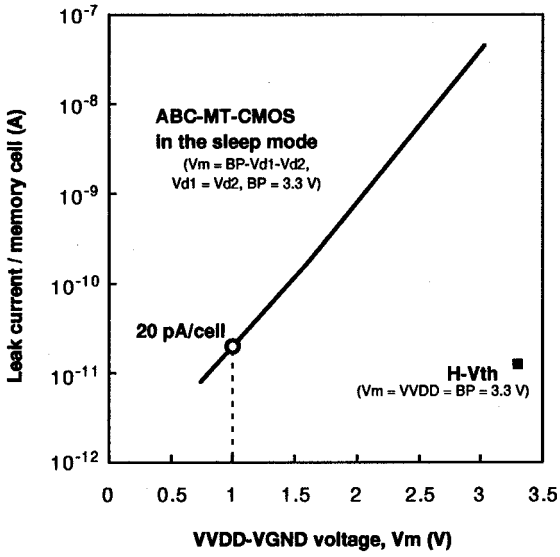

Figure 3 Simulated leakage current for a memory cell

4. CLAMPED SOURCE-LINE AND BIT-LINE SCHEME

The power in the active mode can be divided into dynamic power and static power. The dynamic power arises from the change in the internal level by the change in the input signals. On the other hand, the static power is caused by the leakage current of the transistors, which is independent of the input signals. When the SRAM is activated and being operated, both the dynamic and the static power are consumed. Therefore, the circuit consumes a static power in the active mode even when the input signal does not change. We call this state the "standby mode". The reduction of the static power in the standby mode is an important factor for an SRAM with ABC-MT-CMOS, because the leakage current is large.

We propose the Clamped Source-line and Bit-line scheme (CSB) in order to reduce this undesirable power dissipation in the standby mode. It also contributes to improving the access time by using the simple sense amplifier. A schematic of the read circuit is shown in Fig. 4. A pre-charge and holding circuit, a memory cell and a sense amplifier are shown in the figure. The source line for the p-MOS transistors of the memory cell is clamped by the low-threshold p-MOS transistor Qm, whose gate and drain are common. If we assume that VVDD = BP = 1.0 V and that the clamped voltage, Vms, is 0.2 V, which is equal to the threshold voltage of Qm, the source level of the memory cell becomes 0.8 V. The backgates of the load transistors, p1 and p2, in the memory cell are driven to reverse bias, so that their threshold voltage increase. Figure 5 shows the

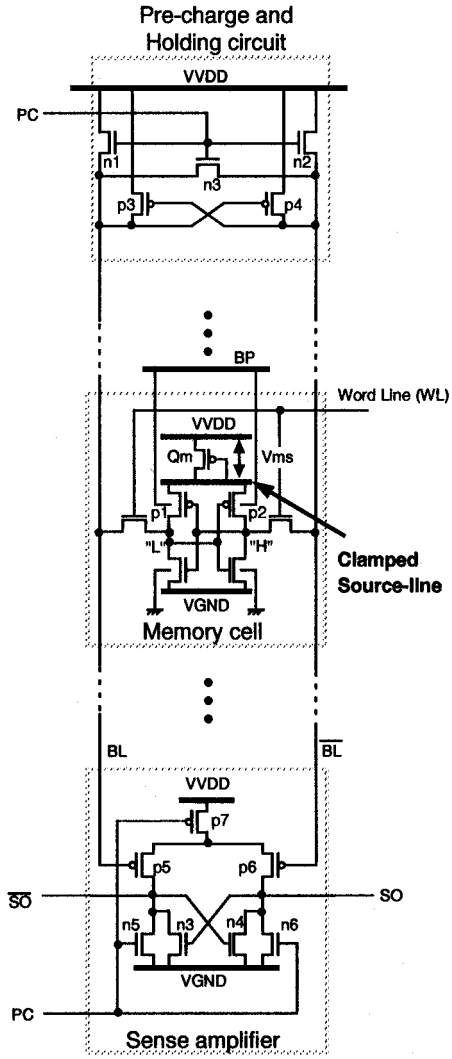

Figure 4 Schematic of read circuit

dependence of the simulated leakage current per memory cell on the clamped source line level, (VVDD - Vms). The leakage current at the Vms = 0.2 V becomes a half of that at Vms = 0 V.

By clamping the source lines, the internal nodes of the memory cell remain at the (VVDD-Vms) and VGND level. In order to ensure the stability of the memory cell in read operations, we clamped the pre-charge level of the bit-lines to the (VVDD-Vms) level. As shown in Fig. 4, the pre-charge circuit consists of the n-MOS transistors n1 and n2 for pre-charging the bit-lines, and n3 for equalizing the bit-lines. The cross-coupled p-MOS transistors, p3 and p4 clamp the bit-lines to the (VVDD-Vms) level. Though n1 and n2 also seem to clamp the bit-lines, they do not decide the bit-line level because their backgates are biased to increase the threshold voltage. The swings of the bit-lines become smaller than without clamping, therefore, the

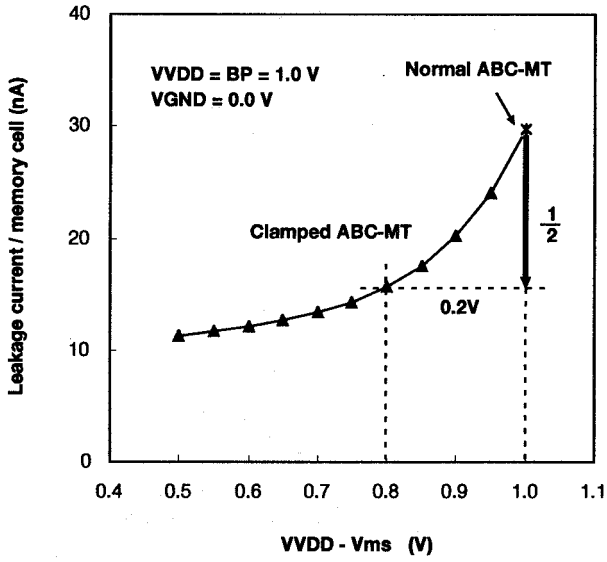

Figure 5 Simulated leakage current against clamped source line voltage (VVDD - Vms)

power of charging and discharging of the bit-lines is reduced. If we assume that Vms = 0.2 V, it is reduced to 80%.

The sense amplifier consists of the transistors, p5 - p7 and n3 - n6. The bit-lines, BL and $\overline{BL}$, are connected to the p-MOS transistors, p5 and p6, respectively, and has the complementary outputs, SO and $\overline{SO}$.

Figure 6 shows the waveforms of this circuit in the read cycle. In the initial condition, the pre-charge control signal PC is at high level. Then both the bit-lines, BL, $\overline{BL}$, are set to (VVDD - Vms) level by the pre-charge and holding circuit. The outputs of the sense amplifier, SO and $\overline{SO}$, are set to the VGND level by the n-MOS transistors Q5 and Q6. After the clock input rises, the pre-charge control signal, PC, goes to low level and the word-line, WL, goes to high level simultaneously. Then if the BL goes down due to the driver transistor of the memory cell, it quickly turn on the transistor p5. Because the pre-charge level of the bit-lines are set to the level just below VDD by Vms, which is equal to the threshold voltages of p5 and p6. The output node, $\overline{SO}$, goes to high level. Then the other output, SO, is forced to VGND level by the transistor, n4. The lowering of BL turns on p4, which makes $\overline{BL}$ go to VVDD level. This makes the leakage current of the transistor p6 cut off. In this way, the read operation completes and the next pre-charge cycle starts. The dashed lines in Fig. 6 show the case when CSB is not used, in which both bit-lines are pre-charged to VVDD level and the source line of the memory cell is not clamped. It is found that the access time of the SRAM with CSB improved from that of a normal SRAM without CSB. The CSB scheme not only reduces the power dissipation of the bit-lines but also achieves high-speed access.

5. 32 K-BIT GATE ARRAY SRAM

In order to evaluate the effectiveness of this work, we designed and fabricated chips containing 32 K-bit SRAMs with 0.35 μm CMOS gate array, triple metal. Figure 7 shows a microphotograph of a chip. The chip size is 6 mm x 5 mm. The size of core area which corresponds to the sea of gate arrays region is 4 mm x 3 mm. All the transistors in the core area have a low-threshold voltage which is 0.12 V for n-MOS transistors and 0.20 V for p-MOS transistors. Here, the threshold voltage is defined as the 1 μA drain current. The high-threshold transistors (Q1-Q4, and D1 and D2) are located into the I/O buffer region with a small area overhead [1]. The high-threshold voltage is 0.53 V for n-MOS transistors and 0.58 V for p-MOS transistors. The total number of n-MOS and p-MOS transistors in the core region is 139K and 73K, respectively, including peripheral circuits. The characteristics of the chip are summarized in Table 1. The size of the SRAM is 1.8 mm x 2.8 mm. Its configuration is 128 bits by 256 words. The memory cell arrays are divided into two planes. Each memory cell array plane has 256 rows by 64 columns. The 128 cells are accessed simultaneously.

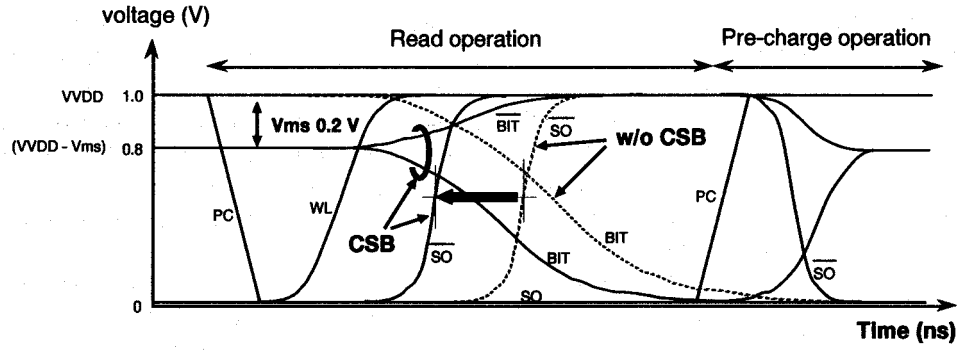

Figure 6 Waveform of a read cycle

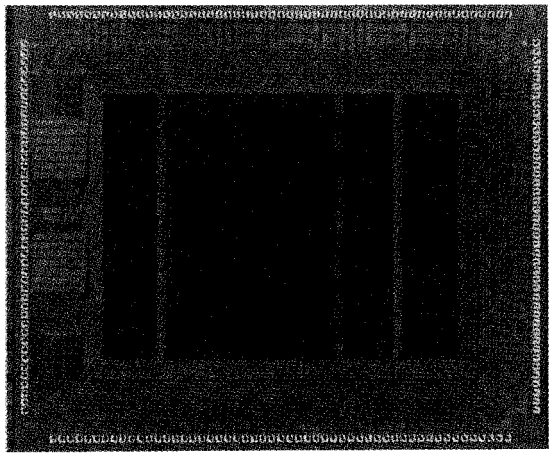

Figure 7 Microphotograph of chip

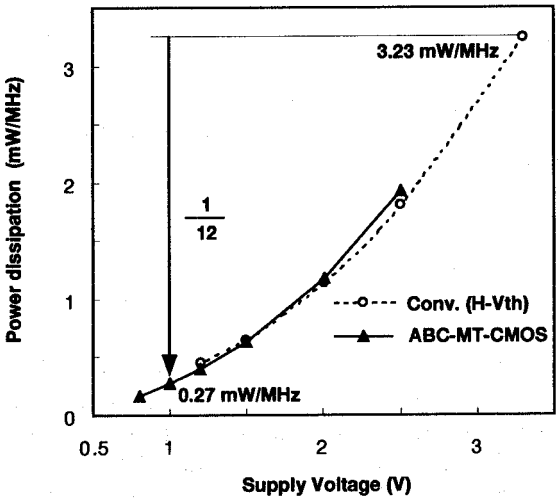

Figure 8 Power dissipation against supply voltage

We then tested the chip. The SRAM passed all the test programs including the march pattern and row bar pattern. It also passed the data retention test in the sleep mode. We compared the active power of the proposed SRAM using ABC-MT-CMOS with the conventional high-threshold SRAM, which we fabricated for the reference. Figure 8 shows a graph of the measured active power dissipation for the supply voltage. The solid line shows the SRAM using ABC-MT-CMOS with the CSB scheme and a dashed line shows the conventional SRAM. The active power of the SRAM is 0.27 mW/MHz at 1.0 V. A conventional SRAM is 3.23 mW/MHz at 3.3 V and cannot operate at 1.0 V. The power is reduced to 1/12 of a conventional SRAM.

Figure 9 shows the measured leakage current of the chip. For a conventional SRAM, which consists of high-

Table 1 Characteristics of chip

Process	0.35 μm CMOS 3-metal
Supply Voltage	I/O 3.3 V Core 1.0 V
High Threshold Voltage	0.58 V (PMOS) 0.53 V (NMOS)
Low Threshold Voltage	0.20 V (PMOS) 0.12 V (NMOS)
Chip Size	6.0 mm x 5.0 mm
Core Size	4.0 mm x 3.0 mm
SRAM configuration	32 K-bit SRAM (128 bit x 256 word)
SRAM Size	2.8 mm x 1.8 mm (5.0 mm^2)
Total SRAM transistors	73 KTr. (PMOS) 139 KTr. (NMOS)

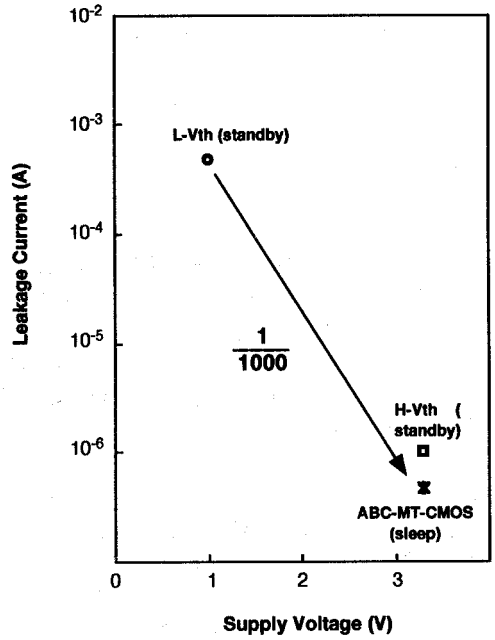

Figure 9 Measured leakage current

threshold transistors, the leakage current is about 1 μA. The leakage current of the ABC-MT-CMOS in the sleep mode is 0.6 μA with a power dissipation of 2 μW. The standby current of ABC-MT-CMOS at 1.0 V is 0.4 mA. The leakage current in the sleep mode is reduced to approximately 1/1000 of the standby mode, which is comparable to a conventional SRAM with 3.3 V power supply.

Figure 10 shows the effect of the CSB scheme on the power reduction of the SRAM in the active mode. We measured the static power and the active power of the SRAMs both with and without CSB. The static power of the SRAM with CSB is 0.4 mW, which is reduced to 40% of the SRAM without CSB. The active power of the SRAM with CSB is

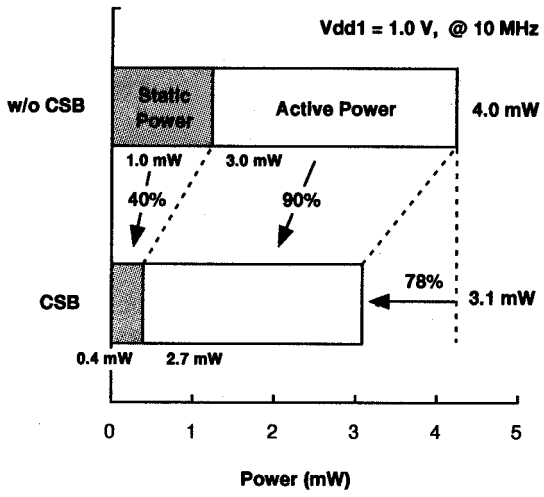

Figure 10 Comparison of power in active mode

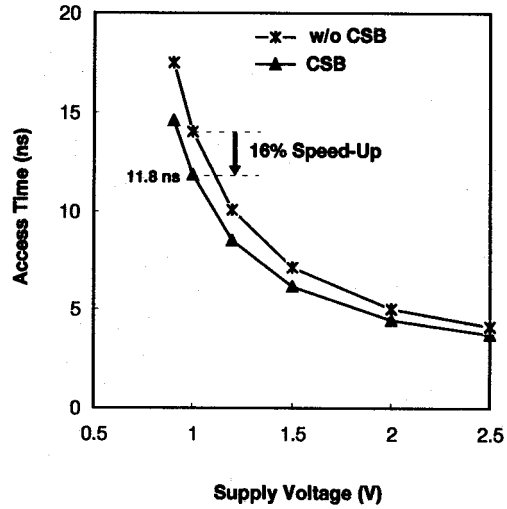

Figure 11 Measured access time

0.27 mW/MHz, which is reduced to 90% of the SRAM without CSB. The total power dissipation of the SRAM with CSB and without CSB at 10 MHz operation are 3.1 mW and 4.0 mW, respectively. The total power is reduced to 78% by the use of CSB.

Figure 11 shows the access times of the SRAM using ABC-MT-CMOS. The access time of the SRAM with CSB is 11.8 ns at 1.0 V, while that without CSB is 14.0 ns. Therefore, the CSB increases its speed by 16% as well as reducing the a power reduction. The minimum operating voltages are 0.8 V for both SRAMs.

6. CONCLUSION

A low power, low voltage SRAM using Auto-Backgate Controlled MT-CMOS has been proposed. Test chips containing a 32 K-bit gate array SRAM were designed and fabricated. It reduced undesirable leakage currents to 1/1000 in sleep mode while retaining the data stored in the memory cells. The active power was reduced to 1/12 compared with a conventional SRAM with a 3.3 V. We have also adopted the Clamped Source-line and Bit-line scheme which reduce the access time by 16% and the power by 22%. We confirmed the effectiveness of this work from the experimental results.

7. ACKNOWLEDGMENTS

The authors would like to thank T. Ohno and A. Maeda for the process development and M. Asai for supporting the evaluation test.

8. REFERENCES

[1] H. Makino et al., "An Auto-Backgate-Controlled MT-CMOS Circuit", submitted to Sympo. on VLSI Circuits, June 1998.

[2] T. Kuroda et al., "A 0.9 V 150 MHz 10 mW 4 mm^2 2-D Discrete Cosine Transform Core Processor with Variable-Threshold-Voltage Scheme", 1996 Dig. Tech. Papers of ISSCC, pp. 166-167, February 1996.

[3] S. Mutoh et al., "1-V Power Supply High-Speed Digital Circuit Technology with Multithreshold-Voltage CMOS ", IEEE JSSC, vol. 30, no. 8, pp. 847-854, August 1995.

[4] S. Shigematsu, et al., "A 1-V high-speed MTCMOS circuit scheme for power-down applications", 1995 Dig. Tech. Papers of Symp. on VLSI Circuits, pp. 125-126, June 1995.

[5] W. Lee, et al., "A 1 V DSP for Wireless Communications", Dig. Tech. Papers of ISSCC, 1997.