True Single-Phase Energy-Recovering Logic for Low-Power, High-Speed VLSI

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Abstract

In dynamic logic families that rely on energy recovery to achieve low energy dissipation, the flow of data through cascaded gates is controlled using multi-phase clocks. Consequently, these families require multiple clock generators and can exhibit increased energy consumption on their clock distribution networks. Moreover, they are not attractive for high-speed design due to clock skew management problems.

In this paper, we present TSEL, the first energy-recovering logic family that operates with a single-phase clocking scheme. TSEL outperforms previous energy-recovering logic families in terms of energy efficiency and operating speed. In HSPICE simulations with a standard 0.5μm technology from MOSIS, pipelined carry-lookahead adders in TSEL function correctly for operating frequencies exceeding 280MHz. For operating frequencies above 80MHz, they dissipate considerably less energy per operation than alternative implementations of the same adder architecture in other energy-recovering logic families. In comparison with their CMOS counterparts, the TSEL adders dissipate about half as much energy at 280MHz. Our results indicate that TSEL is an excellent candidate for high speed and low power VLSI system design.

1 Introduction

Energy recovery is a promising approach to the design of VLSI circuits with extremely low energy dissipation [1, 7, 17]. Energy-recovering logic architectures (a.k.a. adiabatic circuits) achieve low energy consumption by restricting currents to flow across devices with low voltage drops and by recycling the energy stored in their capacitors. In order to control cascaded gates, however, these logic families require multi-phase clocks. Consequently, adiabatic circuits are likely to exhibit significant energy dissipation on their clock distribution networks. Moreover, they are not attractive for high-speed system design due to the plethora of design problems associated with multi-phase clocks.

In this paper, we present TSEL (pronounced *tee'-sel*), a novel single-phase energy-recovering logic geared towards high speed and low energy VLSI design. To our knowledge, TSEL is the first true single-phase energy-recovering logic family. TSEL gates are dual-rail and always present a balanced load to the clock generator, regardless of the particular data computed. High operating speeds and low energy consumption are ensured by a cross-coupled latch structure and two DC reference voltages. Moreover, the TSEL logic family is functionally complete, and TSEL cascades can be implemented straightforwardly in an NP domino style.

We designed and simulated in HSPICE a variety of circuit structures, including pipelined carry-lookahead adders and cascades of complex gates. Our TSEL designs function correctly for frequencies exceeding 280MHz. In comparison with their CMOS counterparts, our TSEL designs dissipate about half as much energy at 280MHz. Moreover, TSEL outperforms previously proposed adiabatic logic families that use a similar cross-coupled latch structure. Specifically, our TSEL circuits dissipate about two thirds as much energy per operation as their corresponding circuits designed in 2N-2P or CAL, the most efficient adiabatic logic families that are still functional at such high speeds.

Several energy-recovering logic families have been proposed in recent years. They all require at least two-phase clocks to control cascaded gates, however. A scheme with asymptotically zero dissipation that requires reversible computations has been described in [17]. Two relatively simple energy-recovering logic styles that use diodes to avoid reversibility were proposed in [8, 12]. Complementary adiabatic MOS (CAMOS) and fully adiabatic MOS (ADMOS) were proposed in [6] for high-speed design. Various logic families that use a cross-coupled latch structure similar to the one in TSEL have been introduced and evaluated in [11, 13, 14, 15, 16]. These logic families include 2N-2P, 2N-2N2P, pass-transistor adiabatic logic (PAL), and clocked CMOS logic (CAL). A 16-bit microprocessor that relies on clock-powered logic to reduce energy consumption has been described in [3, 4].

The remainder of this paper has four sections. In Section 2 we review the operation of the adiabatic logic families most closely related to TSEL. The structure and operation of TSEL gates and cascades are presented in Section 3. In Section 4 we present HSPICE simulation results for pipelined 4-bit carry-lookahead adders that we designed in 0.5μm MOSIS technology. Our results show the superior energetics of TSEL over CMOS and other adiabatic logic families for operating frequencies above 80MHz. We summarize our contributions in Section 5.

2 Overview of Adiabatic Logic Families

This section highlights the operation of static CMOS and several adiabatic logic families related to TSEL. We focus on the characteristics of the adiabatic logic families 2N-2N2D, 2N-2P, 2N-2N2P, PAL, and CAL that use cross-coupled latches in a manner similar to TSEL.

The dominant factor in the dissipation of static CMOS logic is the power required to charge capacitive nodes. In the CMOS inverter of Figure 1, when the power supply drives the output node high, the voltage V_{dd} is applied abruptly resulting in a high voltage drop across the PMOS switching device MP. The total energy drawn from the power supply is $E_c = CV_{dd}^2$, where C is the capacitance of the output node.

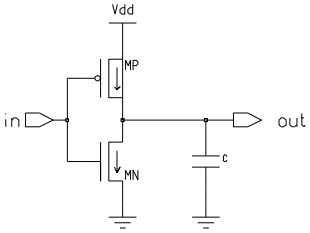

Figure 1: Static CMOS inverter.

Half of this energy is dissipated on the on-resistance R of the device MP, and the other half is stored in the output capacitance. When the output is driven low at a later cycle, the energy stored in the output capacitor is dissipated on the on-resistance R of the device MN.

In contrast to conventional CMOS circuits, adiabatic circuits charge or discharge capacitors while striving to keep the potential drop across their switching devices small. Thus, only a fraction of the energy supplied during each cycle is dissipated on their resistive components. The bulk of the supplied energy is returned to the power supply and can be reused in subsequent cycles. Typically, power supplies for adiabatic circuits provide a time-varying, periodic output signal, or *power clock*, that gradually swings between 0V and V_{dd}. The period of this signal is long enough to maintain a small potential drop V_R. A simple form of adiabatic charging can be accomplished using a power supply with a ramp output. Such a signal can be approximated using a resonant *RLC* oscillating structure. Other adiabatic generator designs have been presented in [2, 5, 17]. The number of power clocks required to control cascaded gates is an important consideration in adiabatic logic design, since it affects energy dissipation, operating speed, and design complexity.

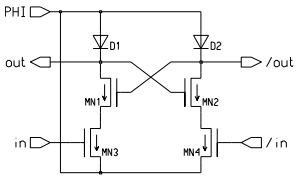

Figure 2: A 2N-2N2D inverter. Cascades require a two-phase power clock. The power-clock line is denoted by PHI.

Figure 2 illustrates 2N-2N2D, an adiabatic logic family that uses diodes in conjunction with a two-phase, nonoverlapping clock to achieve adiabatic charging [12]. Its main drawback is that the diodes impose a lower bound of $E_{diode} = CV_{dd}V_{on}$ on the power dissipation of each gate, where V_{on} is the turn-on voltage of the diode.

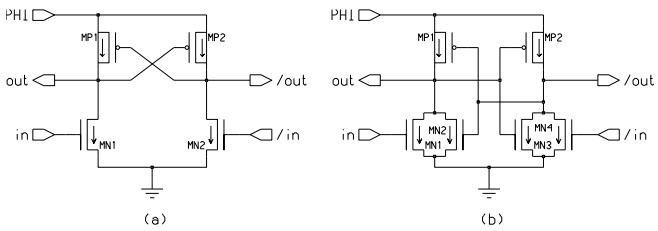

Figure 3: (a) A 2N-2P and (b) a 2N-2N2P inverter. Cascades require four power-clock phases in quadrature.

Figure 3 shows inverters from 2N-2P and 2N-2N2P, two related adiabatic logic families that have no diodes and use four-phase clocks for controlling cascades [13]. These families exhibit a non-adiabatic dissipation proportional to CV_t^2, where V_t is the threshold voltage of the switching devices. The non-adiabatic switching event occurs during a brief interval in the beginning of the evaluate phase and provides the voltage differential that activates a cross-coupled latch structure similar to the one used in the Sample-Set Differential Logic (SSDL) [9]. 2N-2P and 2N-2N2P present a balanced capacitive load and surpass all other adiabatic logic families in speed of operation. The primary advantage of 2N-2N2P over 2N-2P is that the cross-coupled NMOS switches result in non-floating outputs.

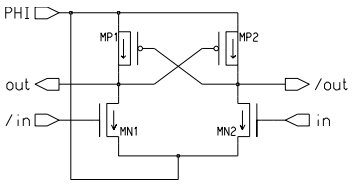

Figure 4: A PAL inverter. In this logic family, cascades require a two-phase power clock.

Figure 4 illustrates an inverter from PAL, an energy-recovering logic family similar to 2N-2P [16]. In PAL, the ground node of 2N-2P is connected to the power supply in order to eliminate non-adiabatic energy consumption. PAL achieves fully adiabatic operation at the cost of high-speed operation. Cascaded PAL gates are controlled by a two-phase clock.

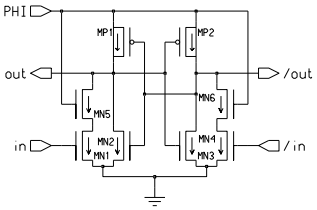

Figure 5: A CAL inverter. Cascades require a single-phase power clock and two nonoverlapping square-wave clocks.

Figure 5 shows an inverter designed in CAL, an energy-recovering logic related to 2N-2N2P [14]. The main structural difference between CAL and 2N-2N2P is the path control switches in the pull-down tree. In CAL, cascaded structures are controlled by a single-phase clock and two auxiliary square-wave clocks. Thus, even though this logic is referred to as single-phase, its cascades are controlled by three waveforms. In terms of their operating speed, CAL gates are comparable to 2N-2N2P gates. CAL circuits achieve half the throughput of corresponding 2N-2N2P circuits, however, because they enable logic evaluation in alternate clock cycles. Moreover, CAL designs tend to be more dissipative than 2N-2N2P, due to the additional devices they use.

3 Operation of TSEL

TSEL is a partially adiabatic logic akin to 2N-2P, 2N-2N2P, and CAL. Power is supplied to TSEL gates by a single-phase clock. Cascades are composed of alternating PMOS and NMOS-type gates. Two DC reference voltages ensure high-speed and high-efficiency operation. They also enable the cascading of TSEL gates in an NP domino style. This section describes the structure and operation of TSEL.

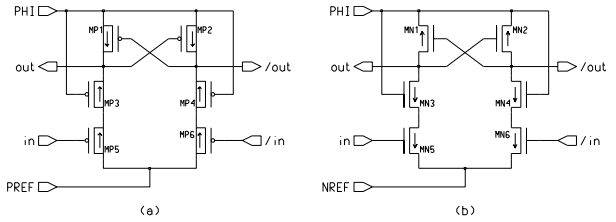

Figure 6: (a) A PMOS and (b) an NMOS inverter in TSEL.

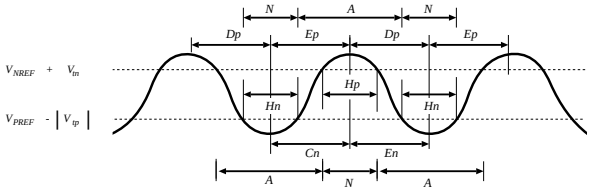

Figure 7: Gate-to-gate timing interface. D_P: PMOS *discharge* phase, E_p: PMOS *evaluate* phase, H_p: PMOS output stable, C_N: NMOS *charge* phase, E_n: NMOS *evaluate* phase, H_n: NMOS output stable, A: adiabatic switching, and N: non-adiabatic switching)

3.1 TSEL PMOS Gate

The basic structure of a TSEL PMOS gate is shown in the PMOS inverter of Figure 6(a). This inverter comprises a pair of cross-coupled latches (MP_1 and MP_2), a pair of current control switches (MP_3 and MP_4), and two function blocks (MP_5 and MP_6). The port PHI supplies the power clock Φ. The port PREF supplies a constant reference voltage V_{PREF}. Inputs and outputs are dual-rail encoded. The main structural characteristics that differentiate TSEL from the other energy-recovering logic families are the current control switches and the reference voltage.

The operation of a TSEL PMOS gate has two phases: *discharge* and *evaluate*. Figure 7 illustrates these phases with respect to the power clock Φ. During *discharge*, the energy stored in the node capacitance of out or $\overline{\text{out}}$ is recovered. Initially, Φ is *high*. As Φ starts ramping down toward *low*, it pulls both out and $\overline{\text{out}}$ down toward the PMOS threshold voltage $|V_{tp}|$. This event is adiabatic until Φ drops below $V_{PREF} - |V_{tp}|$.

During *evaluate*, the output is evaluated. Let us assume that in is *high* and $\overline{\text{in}}$ is *low*. Initially, Φ is *low*. As Φ starts rising, MP_1 and MP_2 turn on. While Φ remains below $V_{PREF} - |V_{tp}|$, MP_3 and MP_4 are conducting. Since V_{PREF} exceeds Φ, a pull-up path is created from PREF to $\overline{\text{out}}$, and the voltage at $\overline{\text{out}}$ starts rising toward V_{PREF}. The cross-coupled latches function as a sense-amplifier and boost the voltage difference of the two output nodes. As soon as this difference exceeds $|V_{tp}|$, MP_1 turns off and the output $\overline{\text{out}}$ is charged adiabatically from that point on.

When Φ exceeds $V_{PREF} - |V_{tp}|$, MP_3 and MP_4 turn off and disconnect the functional blocks from the outputs out and $\overline{\text{out}}$. Hence, any further changes in the inputs do not propagate to the outputs. At the end of the *evaluate* phase, $\overline{\text{out}}$ is charged up to the peak power-clock voltage. The output logic values can be sampled near the peak of Φ. Ideally, the output node out stays at $|V_{tp}|$ throughout the duration of the *evaluate* phase.

3.2 TSEL NMOS Gate

The TSEL inverter in Figure 6(b) shows the basic structure of an TSEL NMOS gate in which outputs are precharged high. The operation of the NMOS gate is complementary to the PMOS one. The two phases in the operation of an NMOS gate are *charge* and *evaluate*. During *evaluate*, a pull-down path is formed from an output to NREF as long as Φ exceeds $V_{NREF} + V_{tn}$. When Φ drops below $V_{NREF} + V_{tn}$, the current control switches disconnect the functional blocks from the outputs, and the recovery of the energy stored in one of the output nodes is initiated. Any further changes in the inputs do not affect the final output values which are sampled near the crest of Φ.

3.3 Cascading TSEL Gates

TSEL cascades are built by stringing together alternating PMOS and NMOS gates. The only signal required for controlling a TSEL cascade is the power clock Φ. A single reference voltage suffices to ensure correct operation. The speed and energy-efficiency of the cascade can be improved, however, by using separate reference voltages V_{PREF} and V_{NREF} for the PMOS and NMOS gates, respectively. To ensure minimal dissipation, these voltages must be tuned depending on the operating frequency. This section describes the operation of TSEL cascades and explains the dependence of their efficiency on the choice of reference voltages.

The relative timing of the gates in a TSEL cascade is shown in Figure 7. At any time during the circuit's operation, either all PMOS gates evaluate and all NMOS gates charge or all PMOS gates discharge and all NMOS gates evaluate. The brief time interval between evaluate/discharge or evaluate/charge during which the outputs of a gate are stable is called the *hold* stage in that gate's operation. While the current switches of the odd stages are off, their outputs are stable. At the same time, the functional blocks of the even stages are connected to the reference voltage and can safely evaluate their outputs. After half a cycle, while the current switches of the even stages are off, the functional blocks of the odd stages are connected to their reference voltage and their inputs are stable.

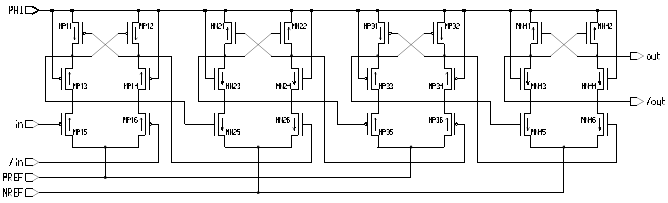

Figure 8: A 4-stage pipeline of TSEL inverters.

A PNPN cascade of TSEL inverters is shown in Figure 8. Figure 9 shows the input/output waveforms obtained from HSPICE simulations of this cascade at 100MHz with a 3V peak power supply and a 0.5μm technology from MOSIS. The input signal was the periodic sequence 01110111 ....

The reference voltages V_{PREF} and V_{NREF} enable the cascading of TSEL gates without any intermediate inverters. These voltages affect the energy dissipation of the TSEL structures, and their optimal values depend primarily on the operating frequency. As V_{PREF} decreases, the non-adiabatic event N has shorter duration, and thus the associated energy dissipation decreases. Symmetrically, as V_{NREF} increases, the energy dissipation associated with the non-adiabatic event in the NMOS gates decreases. Therefore, from an energy dissipation perspective, two reference voltages are preferable to a single reference voltage. In fact, the closer V_{PREF} and V_{NREF} are to 0V and V_{dd}, respectively, the lower the energy dissipation of the TSEL cascade

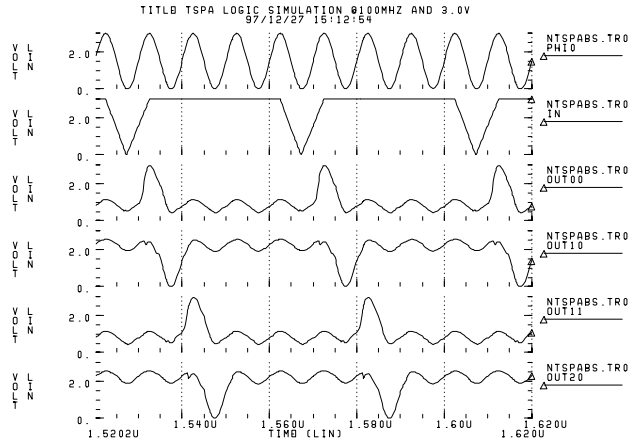

Figure 9: Waveforms obtained from HSPICE simulations of a 4-stage pipeline of TSEL inverters. (1) power clock Φ, (2) input of 1st stage, (3) output of 1st stage, (4) output of 2nd stage, (5) output of 3rd stage, and (6) output of 4th stage.

is. If V_{PREF} drops below a certain value or V_{NREF} exceeds a certain value, however, the *hold* stages become too short, and the cascade fails. Theoretically, the minimum value for V_{PREF} is $2 \cdot |V_{tp}|$, and the maximum value for V_{NREF} is $V_{dd} - 2 \cdot V_{tn}$. For low operating frequencies, the energy consumption of TSEL circuits is minimized by setting V_{PREF} and V_{NREF} to their minimum and maximum values, respectively. Larger reference voltages can be used to speed up the operation of the devices, thus avoiding the area overhead associated with sizing.

4 Simulation Results

We evaluated the performance of TSEL by simulating a variety of circuits we designed in 0.5μm CMOS technology from MOSIS. In our simulations, we compared the energy dissipation of our TSEL designs with equivalent designs developed in other adiabatic or conventional CMOS logic families. We also investigated the sensitivity of the energy consumption in TSEL designs to variations in the reference voltages. In this section, we present simulation results for pipelined 4-bit carry-lookahead adders (CLAs). Our simulations evaluated the dissipation of the gates *only* and did not include the energy consumed on the clock distribution network or the power clock generator. Since TSEL uses only one clock phase, it is expected that it will be even more efficient when compared with the other adiabatic families that require multi-phase clocks.

The TSEL version of our pipelined 4-bit CLA is shown in Figure 10. The TSEL gates used in this adder are shown in Figures 11 and 12, respectively. Figure 13 gives the waveforms on the critical path of the CLA. For all stages, the output waveforms are fairly stable and demonstrate the promise of TSEL for high-speed, low-energy systems.

We compared the performance of our TSEL adder with equivalent adiabatic adders developed using the 2N-2P, PAL, and CAL logic families. All these families use a cross-coupled latch structure similar to the one in TSEL and can be implemented in a standard technology. We also compared our TSEL circuits with their static CMOS counterparts.

Figure 14 gives the per-cycle energy consumption of our

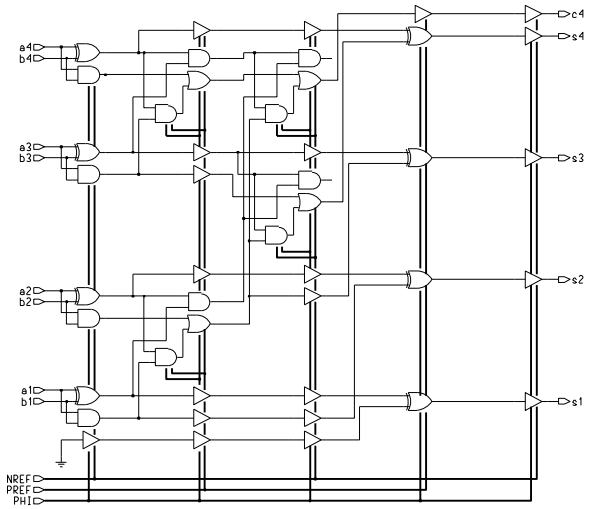

Figure 10: Schematic of a pipelined 4-bit CLA in TSEL.

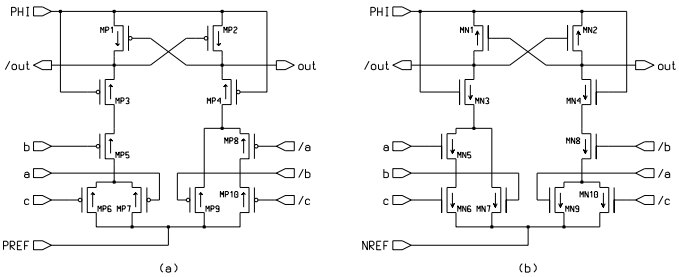

Figure 11: Implementation of out=ac+b in TSEL.

designs as a function of their operating frequency. The peak power-clock voltage was 3V, and each primary output was connected to a 60fF load. As expected, the energy consumption of the static CMOS implementation does not vary with the operating frequency. PAL has the lowest energy dissipation for low operating frequencies but breaks down at around 80MHz. TSEL is dissipative in low frequencies due to the relatively slow switching of the current switches. For operating frequencies above 100MHz, however, TSEL dissipates less energy than any other logic family. At high frequencies, CMOS and CAL do not swing fully from 0V to V_{dd}. On the other hand, 2N-2P and TSEL operate at full logic swing for frequencies up to 280MHz. At 280MHz, TSEL is about 2 times more energy-efficient than static CMOS and about 1.5 times more efficient than 2N-2P and CAL.

Figure 15 shows the flow and dissipation of energy for a 2-input XOR TSEL PMOS gate during a single evaluate/discharge cycle. The operating frequency is 280MHz,

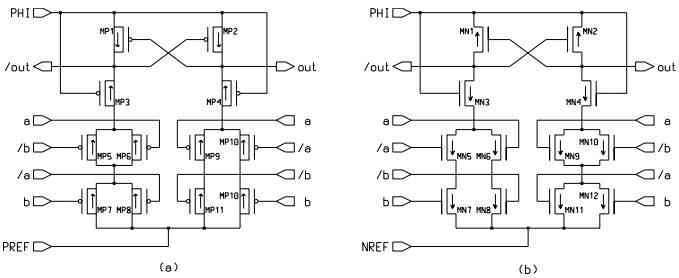

Figure 12: Implementation of out=$a\bar{b} + \bar{a}b$ in TSEL.

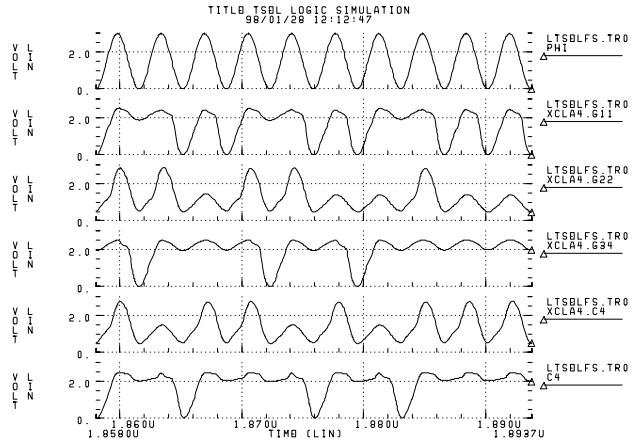

Figure 13: Waveforms along the critical path of a pipelined 4-bit TSEL CLA at 280MHz with 3V peak power clock voltage. (1) power clock Φ, (2) output of 1st stage, (3) output of 2nd stage, (4) output of 3rd stage, (5) output of 4th stage, (6) output of 5th stage.

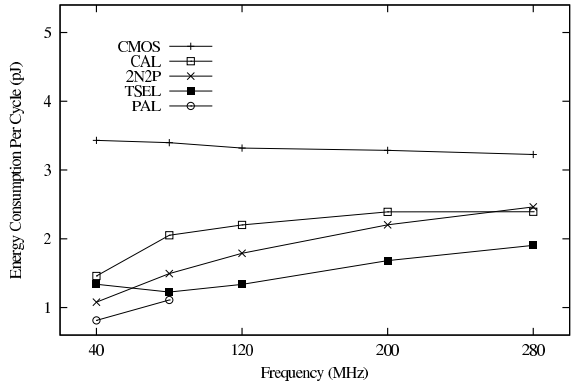

Figure 14: Energy consumption vs. frequency for 4-bit CLA.

and the load at each output is 15fF. The top graph gives the power supplied to the gate by the power clock and the reference voltage line, the power dissipated by the gate's resistors, and the power stored in the gate's output load. Negative power supply denotes energy flowing into the gate, whereas positive supply signifies recovered energy. The bottom graph gives the total energy supplied and the energy dissipated as a function of time.

Figure 16 gives the energy consumption of our designs as a function of the peak power-clock voltage. These results were obtained with the original adder designs that were tuned for a 3V peak power-clock supply. In general, TSEL is more energy-efficient than the other designs. The CAL adder achieves comparable dissipation with TSEL at 2.7V. Its logic swing and throughput are half of the TSEL adder, however.

For each operating frequency in our simulations, the reference voltages V_{PREF} and V_{NREF} were tuned optimally for that specific frequency. For a clock frequency of 200MHz and a 3V peak power-clock voltage, for example, V_{PREF} was set to 1.42V and V_{NREF} was set to 1.74V. Dissipation can be reduced even further by using multiple reference voltages, each one tuned to a particular type of gate. The extent

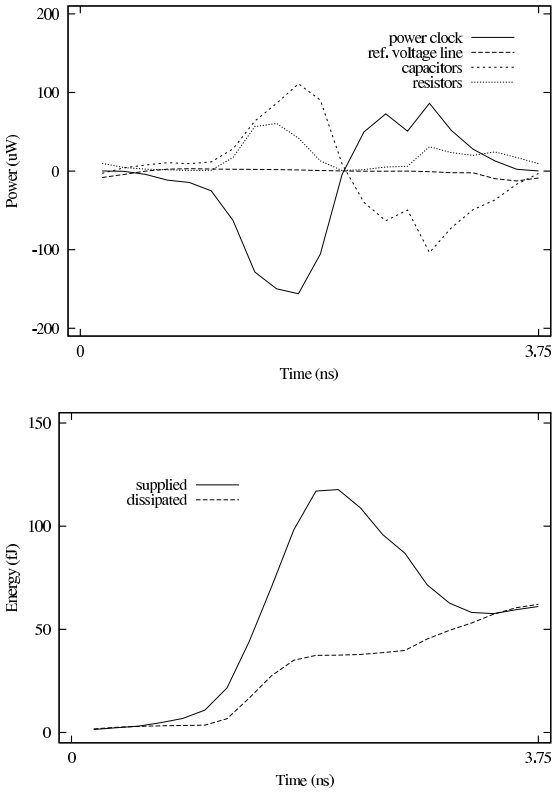

Figure 15: Energetics of a TSEL XOR gate at 280MHz.

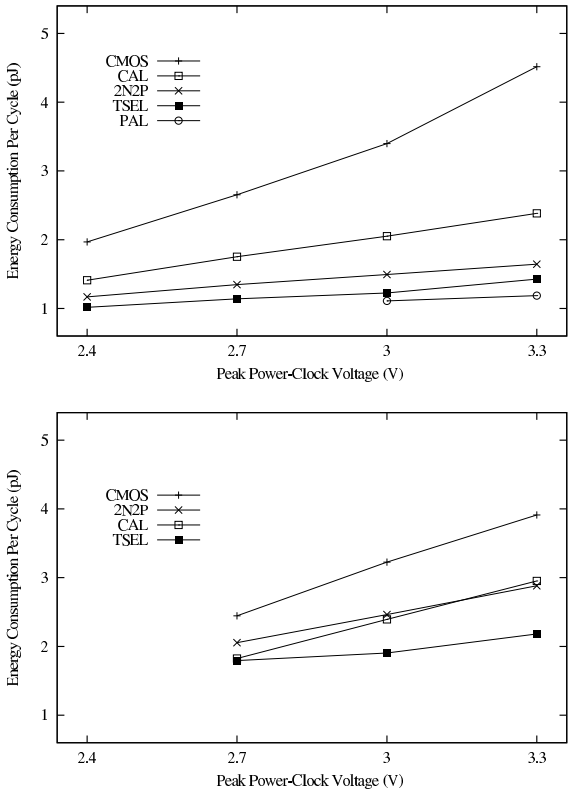

Figure 16: Energy consumption vs. peak power-clock voltage for 4-bit CLA. The operating frequency is 80MHz in the top graph and 280MHz in the bottom graph.

to which the use of more than two reference voltages can improve energy consumption is a topic of further research.

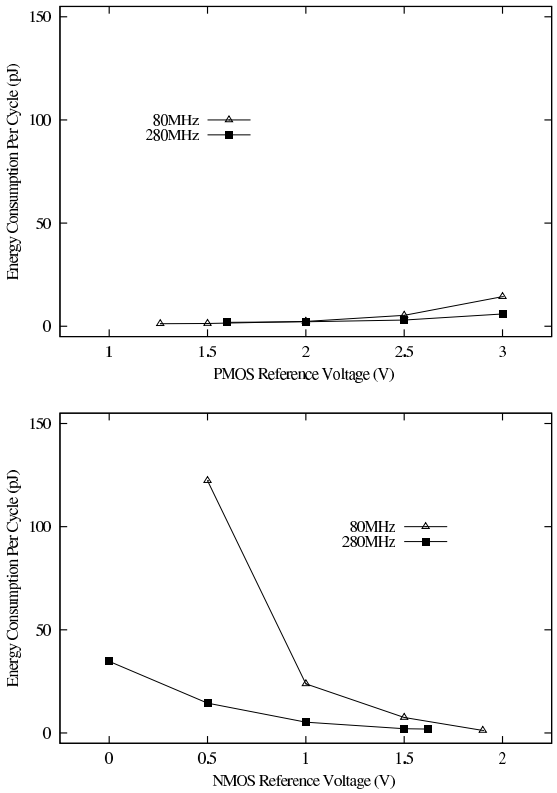

Figure 17: Sensitivity of energy dissipation to reference voltage variations at 80MHz and 280Mhz.

Figure 17 gives the sensitivity of the energy consumption of the 4-bit CLA to variations in V_{PREF} and V_{NREF}. These graphs suggest that the energy efficiency of TSEL is fairly immune to reference voltage variations. For high operating frequencies, sensitivity is extremely low for both PMOS and NMOS. For low operating frequencies, however, TSEL consumption is fairly sensitive to variations in V_{NREF}.

5 Conclusion

We presented TSEL, the first true single-phase energy-recovering logic family. TSEL avoids numerous problems associated with multiple clock phases, including increased energy dissipation and layout complexity in the clock distribution network, clock skew, and multiple AC power supplies.

In HSPICE simulations with a standard 0.5μm MOSIS technology, a 4-bit pipelined CLA in TSEL outperformed corresponding implementations in 2N-2P logic, pass-transistor adiabatic logic (PAL), clocked CMOS adiabatic logic (CAL) and static CMOS logic. TSEL achieves very low energy operation, particularly at high operating speeds. Overall, our investigation shows that TSEL is an excellent candidate for high speed and low energy electronic systems.

Acknowledgments

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