CMOS VCOs for Frequency Synthesis in Wireless Biotelemetry

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1. ABSTRACT

A new phase noise model was used to optimize a differential ring VCO for minimum power consumption. We compare the phase noise performance of three buffer stages using clamped, symmetric and cross-coupled loads, respectively. We propose a cross-coupled buffer topology that achieves lower phase noise by exploiting symmetry. Measured phase noise for a 1.2mW, 150MHz VCO fabricated in 0.5μm CMOS is -103.9dBc/Hz at 500KHz offset, showing good agreement with the theory.

1.1 Keywords

Cmos, frequency synthesis, phase noise, ring oscillator, vco

2. INTRODUCTION

The most important parameters of an implanted biotelemetry system are size and power dissipation. A significant portion of the power budget for any implantable telemetry system is allocated to the generation of the RF carrier. Given the need for small, low-power wireless devices for biotelemetry, a low-power, integrated frequency synthesizer is required.

Figure 1 shows the block diagram and power budget for a CMOS PLL synthesizer used in microprocessor clock generation [1]. The major sources of power dissipation are the VCO (73%) and the frequency divider (22%). The VCO's power dissipation is determined by the frequency of operation and the phase noise performance required. In biotelemetry, low data rates and wide channel spacing relax the phase noise requirement, making phase noise at a 500KHz offset a valid measure.

3. VCO DESIGN

Phase noise performance of a synthesizer is a function of the phase noise of the VCO. The Hajimiri phase noise model [2],

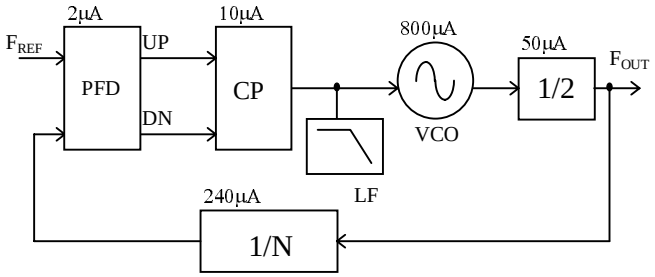

Figure 1. Typical PLL frequency synthesizer power budget

[6] was used to minimize the power dissipation of the VCO.

Phase noise in the $1/f^2$ region is due to white device thermal noise (Figure 2). For a differential ring oscillator using short-channel devices, one may derive the following lower bound on the single-sideband phase noise in the $1/f^2$ region:

$$L\{\Delta f\} = 10 \cdot \log\left\{\frac{18kT}{\pi^2 I_{DD}} \cdot \left(\frac{2.5}{E_C L_{EFF}} + 1\right) \cdot \left(\frac{f_o}{\Delta f}\right)^2\right\}, dBc/Hz \quad \textbf{(1)}$$

where I_{DD} is the tail current of a single stage, E_C is the critical field in silicon, and L_{EFF} is the gate length of the differential-pair devices.

Phase noise in the $1/f^3$ region is due to device $1/f$ noise. It is usually assumed that the $1/f^3$ corner frequency is the same as the $1/f$ corner of device noise. This is not true, as the $1/f^3$ corner is actually given by:

$$f_{1/f^3} = f_{1/f} \cdot \left(\frac{c_o}{2\Gamma_{rms}}\right)^2 \quad \textbf{(2)}$$

where c_0 is the DC Fourier coefficient and Γ_{rms} is the RMS value of $\Gamma(x)$, the impulse sensitivity function (ISF). The ISF accounts for the time-variant sensitivity of the oscillator to its noise sources. The upconversion of device $1/f$ noise occurs through c_0, the DC value of the ISF. However, the DC value of the ISF is governed by the symmetry properties of the single-ended output waveform. This model thus predicts the upconversion of $1/f$ device noise into close-in phase noise as a function of the symmetry of the output waveform.

To start the design, we plotted a series of phase noise curves (Figure 3) for a typical 0.5μm CMOS process ($f_{1/f}$=*3MHz*). We selected the 100μA curve, for a total current drain of 400μA at 200MHz for the VCO core.

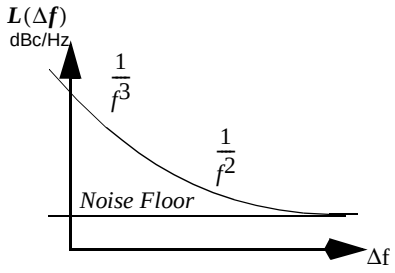

Figure 2. Oscillator close-in phase noise due to upconversion of thermal and *1/f* device noise

The VCO consists of a 4-stage ring oscillator (Figure 4) that uses differential buffer delay stages with replica-feedback biasing [3]. Frequency control is achieved by changing the biasing of the buffer stages which determines the delay through each cell. The layout of the ring oscillator is symmetrical and load balanced to avoid any skewing between the phases. Three ring oscillators were designed, each using a different load circuit for the delay buffer stage: VCO_1-clamped load, VCO_2-symmetric load, and VCO_3-cross-coupled load, respectively.

The clamped-load differential buffer (Figure 5a) used in VCO_1 has excellent noise and PSR characteristics [4]. The cross-coupled diode loads clamp the output swing making the buffer delay insensitive to common-mode noise. Symmetric load buffers (Figure 5b), as used in VCO_2, also have very good supply noise rejection characteristics and have been used extensively in PLL and clock generator designs [5].

For the proposed cross-coupled load (Figure 5c) design of VCO_3, we started with a symmetric load stage with no cross-coupling and swept the width of the cross-coupling devices while maintaining the total width (capacitance) of the loads constant. The maximum symmetry of the output waveform was observed when the widths of M_1 and M_2 were equal to half the width of M_3.

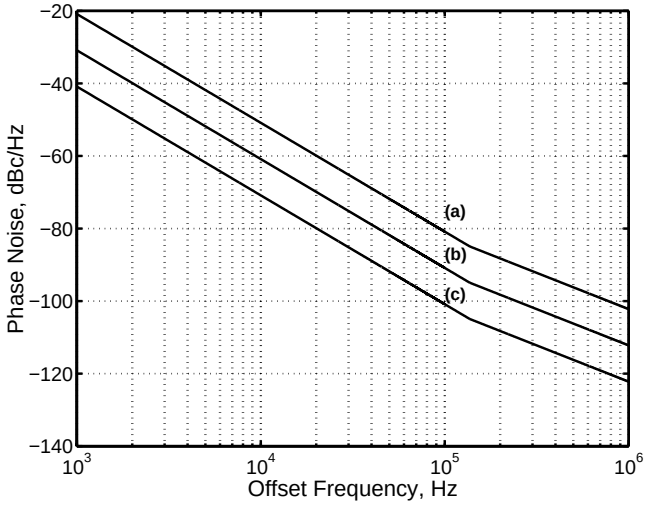

Figure 3. Lower bound on phase noise for ring oscillator at 200MHz for: (a) I_{DD}=10μA, (b) I_{DD}=100μA, (c) I_{DD}=1000μA

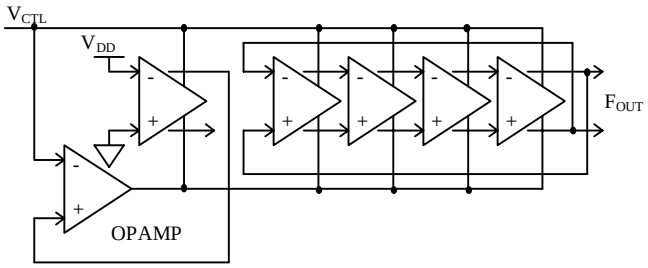

Figure 4. Differential ring oscillator VCO with replica bias

4. SIMULATION AND MEASUREMENTS

To compare the three topologies, a more detailed noise analysis was performed. The predicted noise for a 4-stage oscillator is given by:

$$L\{\Delta f\} = 10 \cdot \log\left\{\left(\frac{\Gamma_{rms}}{\pi V_{swing} C_{node} \Delta f}\right)^2 \cdot \frac{\overline{i_n^2}}{\Delta f}\right\}, dBc/Hz \qquad \textbf{(3)}$$

where $\overline{i_n^2}/\Delta f$ is the total noise contribution from all sources at the output node, C_{node} is the total capacitance at the output node, and V_{swing} is the voltage swing across C_{node}. Figure 6 shows the predicted phase noise for VCO_1, VCO_2, and VCO_3. The $1/f^2$ regions are within 2.6dB of each other as it is to be expected for similarly sized noise sources. The model also predicts lower phase noise in the $1/f^3$ region for VCO_3 as it has better symmetry than the other two.

A test chip was fabricated through MOSIS using the HP 0.5μm CMOS process. The VCO_1 voltage-to-frequency transfer characteristics was measured for different supply voltages (Figure 7). Test results for VCO_1 are shown in Figure 7 for operation at 150.9MHz, along with the phase noise predicted by the model. The phase noise was measured at -103.9dBc/Hz for a 500KHz offset which is very close to the predicted value of -103.2dBc/Hz (Figure 8). These results are well within the 2dB measurement accuracy of the RDL NTS-1000A instrument used.

5. CONCLUSION

To minimize power dissipation of the VCO, a design technique based on a new phase noise model was presented. We have demonstrated a 150MHz VCO fabricated in a standard CMOS 0.5μm process. Measurements of phase noise show good agreement with the theory. We also compared the phase noise performance of three differential buffer stages. We proposed a cross-coupled load buffer that achieves lower phase noise in the $1/f^3$ region well below 500KHz by exploiting single-ended symmetry in the oscillator's waveform.

6. ACKNOWLEDGEMENTS

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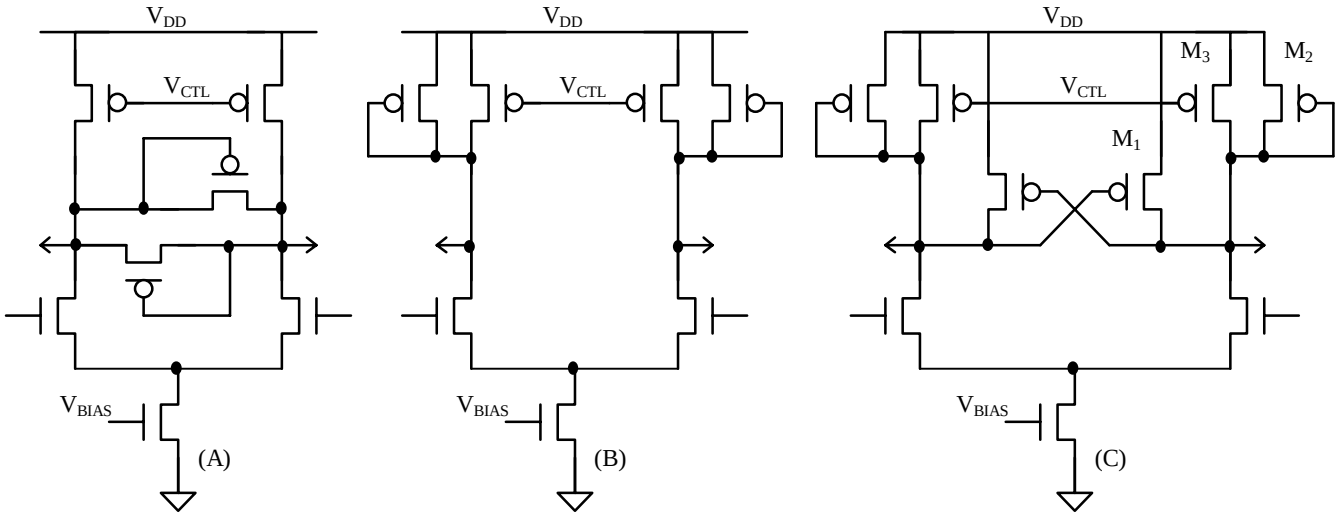

Figure 5. Differential delay buffer cells: (a) VCO_1, clamped-load; (b) VCO_2, symmetric load; (c) VCO_3, cross-coupled load

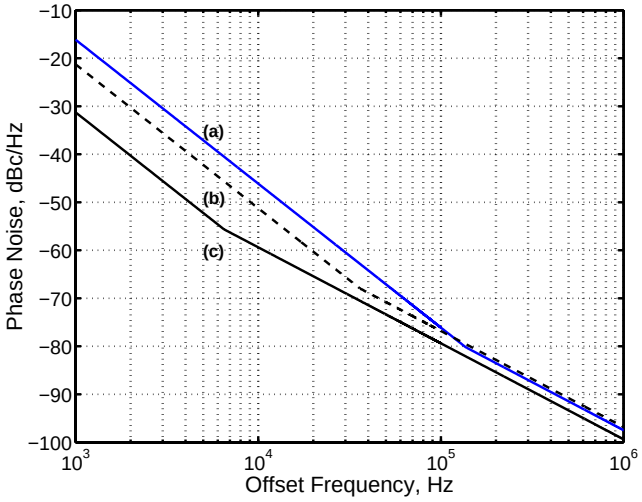

Figure 6. Predicted single-sideband phase noise: (a) VCO_1, (b) VCO_2, (c) VCO_3

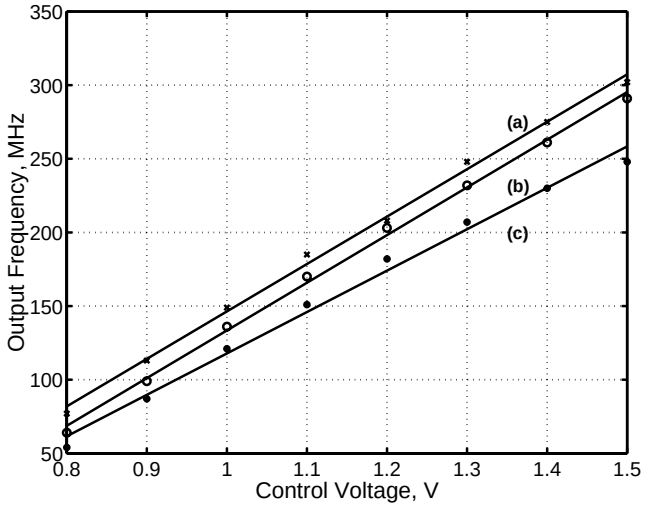

Figure 7. Frequency vs. voltage characteristic for VCO_1: (a)V_{DD}=3.0V, (b)V_{DD}=2.7V, (c)V_{DD}=1.8V

7. REFERENCES

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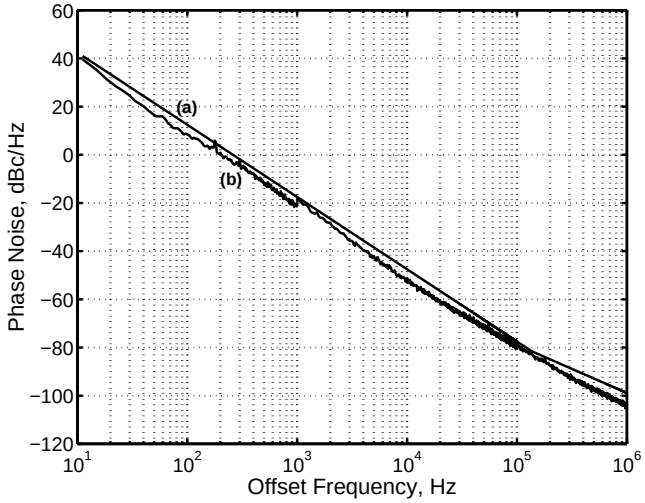

Figure 8. Single-sideband phase noise for VCO_1 at 150.9MHz: (a) predicted, (b) measured