Low Power Salient Integration Mode Image Sensor with a Low Voltage Mixed-Signal Readout Architecture

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1. ABSTRACT

CMOS image sensors are very suitable for battery-operated camera systems due to their low power nature. In this research work, a salient integration mode CMOS image sensor pixel design which requires only 1 or 2 transistors per pixel and a low power readout architecture was developed in a 0.35 μm CMOS technology. High fill factor and small pixel size are achieved at the same time for the 2T pixel design. The readout architecture includes a low voltage low power multi-stage analog data buffer which works as a differential to single-ended conversion mechanism for a new correlated double sampling method. Total data bandwidth and switching power are also greatly reduced. The architecture was developed to be scalable to 0.18 μm technology with 1.2 volt supply voltage, and lower. An experimental chip in an array size of 256×256 with a pixel size of $6.3\mu m \times 6.3\mu m$ was fabricated at a HP's 0.35 μm CMOS technology. Promising experimental results strongly indicates that the new pixel design and readout architecture are suitable for low voltage CMOS camera chips in future generations of CMOS technology.

1.1 Keywords

Salient integration mode image sensor, active pixel sensor, CMOS imaging, low power mixed-signal design, deep submicron technology.

2. INTRODUCTION

CMOS image sensor is becoming increasingly important because the degree of electronics integration achievable on the focal plane. This can enable design of low power camera systems that simplify instrument and system interface [1]. Charge-coupled devices (CCD's) are currently the dominant technology for electronic image sensors. CCD image sensors have the features of high-fill factor and small pixel sizes. Some signal processing operations have been demonstrated with charge-domain circuits [2-3]. However, there are many concerns for CCD such as high power dissipation for large array (2-3 W), smear, and susceptibility to radiation damage. Additionally, it is not easy to integrate CCD's with CMOS circuits for more practical applications due to the additional fabrication complexity and increased cost.

The active pixel sensor array designs originated from California Institute of Technology [7] requires 4 transistors inside a photo-gate pixel to provide low noise and electronic shuttering features. The power consumption for a photo-gate sensor may not be significantly lower than CCD sensor because of the large capacitance on the photo-gate and its transistor count limitations for pixel miniaturization. Many CMOS sensor designs [4-6, 9-10] use three transistors and a photo-diode having a fill factor is around 30% to 40%.

The key issues for pixel miniaturization are the reduction of the number of transistors to improve fill factor and the reduction of the photo-sensitive area in a pixel. Deeper sub-micron technology provides the opportunity to reduce pixel size through reduction of the transistor size and also the area of the photo-sensitive element. Yet, there are many challenges ahead. To reduce the transistor area dramastically, it requires a new pixel structure of fewer transistors and a new corresponding readout architecture. The proposed new pixel structure is operated in salient integration mode which uses the supply voltage swing as much as possible. It is named salient integration mode pixel because the pixel output amplifier is put in a disabled mode while the pixel is accumulating electrons. When the image signal is mature, the pixel output amplifier is operated in readout mode to allow the signal to be sensed. Therefore, the salient integration mode pixels will have a significantly higher fill factor than the active pixel sensors described in [4-7,9-10].

For low voltage low power technology, the supply voltage can be so low that the cascaded op-amp designs are no longer suitable. In order to make the image sensor compatible with at deep sub-micron process technology, a multi-stage signal buffer with differential to single-ended conversion circuit and gain improvement circuit is designed. To further reduce the power consumption on the readout path, a multiplexed multiple bus is also used on the prototype chip design to minimize the total signal bus capacitance.

In the next section, a detailed description on the salient integration mode CMOS pixels is given. It is followed by the low voltage/low power readout architecture. The readout

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architecture is designed suitable to be scaled down to 0.18 μm technology. Detailed study on the technology scaling issues for the pixel design and readout architecture is then provided. The prototype chip design and experimental results are included to demonstrate the function of the image sensors, and its compatibility with future technology.

3. SALIENT INTEGRATION MODE CMOS IMAGE SENSOR

A salient integration mode pixel is a capacitively pulsed CMOS image sensing pixel. By handling pixel selection pulse in a novel fashion, it is possible to reduce the number of transistor in a pixel down to one or two. The circuit schematics of a 2-transistor CMOS salient integration mode active pixel sensor with high threshold voltage transistor as the output amplifier is shown in Figure 1 (a). It includes a reset transistor M_1, a output amplification transistor M_2, a selection pulsing capacitor C_1 and a light collecting diode D_1. The V_{reset} is a reset voltage level. The *COL* wire is the output bit line. *SEL* is the pixel selection wire. M_2 has a higher threshold voltage than M_1 in order to allow the salient integration-mode operation which means performing electron accumulation below the threshold voltage of the output amplification transistor. The capacitor is physically laid out as a poly-silicon layer over the diffusion layer of the diode. Therefore, no any extra space is required to implement this. The cross-sect diagram for a pixel is shown in Figure 2. Notice that the pulse signal (*SEL*) and the bias pulsing capacitor (C_1) can be laid out as a polysilicon layer over the N-island diffusion layer.

The operation of a salient integration-mode pixel can be characterized by the timing diagram as shown in Figure 1 (b). It can be described in 4 major steps. For the first step (1), the signal node is set to a "reset" level which is determined by V_{reset} and the switching condition of the transistor M_1. At the same moment, the *SEL* line is held at its high level (V_{dd}). After the signal node settled at that voltage level, the *RESET* signal is switched to a voltage level $V_{R,low}$ above the substrate potential. By doing, the transistor is kept in an "off" condition but it will be activated if the voltage level of the signal node drops below $V_{R,low}$ - V_T. Such a setup can prevent the forward bias condition of the photodiode. This is used to prevent the blooming effect on the signal node which might cause white spots in an output image.

For the second step (2), the *SEL* line is switched from the high voltage level to a low voltage level. Therefore, the charge being pulled away from the capacitor is

$$\Delta Q = C_1(V_{SelHi} - V_{SelLo}). \quad (1)$$

Due to the capacitive coupling effect, the voltage level of the bottom plate of the capacitor will be pulled down to a level lower than the threshold voltage of the transistor M_2 enabling salient integration-mode operation. In order to achieve better signal range, the threshold voltage of M_2 is adjusted higher than that of M_1.

For the third step (3), the pixel starts to accumulated signal (electrons) on the N-island due to the photo-effect. This is called the salient mode integration. If the pixel is over-exposed, then the anti-blooming function will be activated through the transistor M_1. Therefore, such a pixel will not suffer the over-exposure problem due to strong light condition or other reasons.

At step (4), the same amount of charge ΔQ is restored back to the coupling capacitor. Therefore, the voltage level of the signal node is pull back to a level above the threshold voltage. This pixel is now driving the column bus. The pixel should be held stable to allow the readout circuitry to sample the signal level.

After the signal level is sampled, the *RESET* signal is pulse to high again to reset the pixel. Then, the pixel is held stable again to allow the readout circuitry to sample the reset level. At this time, the pixel is ready to perform a operation for the next integration cycle. This reset transistor can further be replaced by a reset diode to further reduce the size of a pixel for a single transistor pixel design. Normally, if a N-Well process is used, a P-island to N-Well diode can be used as the reset diode. If the N-Well spacing is small enough, the one transistor can be naturally smaller than the 2-transistor pixel. If there is a need to shutter the pixel, the SEL is set to its low level and, thus, the pixel is shut-down from the column bus. This is the electronic shuttering feature. The layout of a 2-transistor pixel and a one-transistor pixel for a 0.35 μm CMOS technology are shown in Figure 3 (a) and (b) respectively.

4. LOW VOLTAGE MIXED-SIGNAL HIGH SPEED SENSOR ARCHITECTURE

In [7], the readout circuit consists of a source follower in the pixel, two sample and hold circuits and two source followers in the column, and one more source follower in the chip output stage. Due to the repetitive use of source follower and body effect of the transistors, the voltage signal attenuates significantly. If three stages of source followers are used, a gain of 0.6 to 0.75 can be normally expected for most of the existing CMOS process technology. Besides, the column access time for a sensor depends very much on the settling time of the column level signal amplifier. If a PMOS based source follower is used, as it was in [7], it takes very large column access time. In fact, due to the large capacitive loading on the column bus, this design is not very effective.

The overall block diagram of the proposed analog bufferis shown in Figure 4. Let us consider the analog signal buffer at each column level for example, the input for the analog signal buffer comes from the pixel output. The pixel output circuit is a source follower. The output channel is time-multiplexed. Therefore, we can formulate the output symbols as

$$V_{SC} = A_{pix}(V_{SP} - \Delta V_{TP}), \quad (2)$$

$$V_{RC} = A_{pix}(V_{RP} - \Delta V_{TP}), \quad (3)$$

where, ΔV_{TP} is the threshold voltage variation on the pixel, V_{SP} is the pixel signal level, V_{RP} is the pixel reset level, V_{SC} is the column signal level, and V_{RC} is the column reset level. Because of the threshold variation and the fixed pattern noise (FPN) in the pixel, double sampling is implemented through the difference of equaiton (2) and equation (3). Due to the weak driving capability of the current bias transistor in the source follower, the PRE_DISCHARGE switch, as shown in Figure 4, is necessary. The pre-discharge signal is activated at the beginning of the row access cycle so that all of the readout access becomes a pull-up operation. The pull-up transistor in a pixel can be optimized to provide the best performance.

The circuit schematics of the low voltage multi-stage analog signal buffer is shown in Figure 5. The proposed analog signal buffer convert the differential signal pair into singled-ended (DTS) format. The output symbol D_1 of the proposed analog signal buffer can be formulated as

$$D_1 = A_{COL}(V_{SC} - V_{RC}) + V_{offset}$$
$$= A_{COL}(A_{pix}(V_{SP} - V_{RP})) + V_{offset} \quad (4)$$

where A_{COL} is the column level gain and V_{offset} it the offset voltage of the analog buffer. The gain factor A_{COL} can be decided by the gain values of the three stages inside the analog buffer.

$$A_{COL} = A_{DTS}A_{SF}A_{Gain}. \quad (5)$$

where A_{DTS}, A_{SF} and A_{gain} are the gain for the DTS stage, source follower, and the current stage respectively. The lumped up gain factor for the whole circuit in Figure 5 can be easily adjusted to be higher than 1. In addition to the gain compensation nature, the device size of the MN3 and MP5 can be decided so that they can drive the output bit line in very short time. This can greatly increase the frame read-out rate.

The offset voltage exists because of the device mismatch, V_T variation and many other reasons. If order to remove the offset voltage, a second symbol D_2 can be sampled at the output with common mode connection at the input of the analo buffer.

$$D_2 = V_{offset}, \quad (6)$$

Then, the pixel signal can be obtained by the difference:

$$V_{pix} = D_1 - D_2. \quad (7)$$

Since the DTS stage convert the differential format into single-ended format, the number of output symbols for the analog buffer is 2 instead of 4 which is used for many APS implementations [1, 5]. The output data bandwidth requirement is reduced by a factor of 2.

The output of such an analog buffer can be connected to a multiplexed multi-bus structure as shown in Figure 4 by another switch with smallest transistor size to reduce the total capacitance of a single bus line. Since the total capacitance on a bus is greatly reduced, the access time is greatly reduced. The total column access time versus pixel count on a bus, through HPSPICE simulation, is shown in Figure 6. It is clear that, from Figure 6, the column access time grow in almost squarely with the number of column. The new read-out design has more than 3 times speed advantage over the design in [7]. And the use of multiplexed multiple bus really makes a lot of difference in the column access time.

5. VOLTAGE AND TECHNOLOGY SCALING ON THE DESIGN

There are several issues involved for technology scaling. First, the photo-sensitive element must maintaingood signal to noise ratio (*SNR*). Second, the pixel structure must be suitable for technology scaling. Third, low voltage low power mixed signal design for the readout signal path is required.

The signal to noise ratio (*SNR*) on the photo-sensitive element on a pixel defines the quality of a pixel. It is a time-dependent variable as the indicator of pixel signal quality over time. In Figure 7, it shows the relationship of the signal level and the noise floor. The total charge Q accumulated on a photon collection node is a function of light intensity (I), quantum efficiency (QE), area (A) and integration time (t). With the diode capacitance as the charge to voltage conversion mechanism, the output voltage (signal level) of a pixel can be described as

$$V_{out} = A_{pix}\frac{QE}{C_{pix}}P(I, A, t), \quad (9)$$

where P is the total number of photons striking on the surface of a pixel and $Q = QE \cdot P$ and A_{pix} is the gain factor of the pixel source follower. The sensitivity can be defined using this methodology as well. To improve the sensitivity, it can be required to put some signal amplification stages at the readout path. The resulting output voltage can be described as

$$V_{out} = A_{AO}A_{col}A_{pix}\frac{QE}{C_{pix}}P. \quad (10)$$

The flat top of the pixel output voltage, Figure 7, indicates the pixel output voltage reached a certain saturation level because of the source follower output limitation.

Measured photon-voltage transfer curve from a CMOS image sensor chip is shown in Figure 7(a). It shows that the knee point of the sensor is smoother than most CCD sensors. In order to explain the technology scaling effect on the pixels, an mathematical model is constructed as shown in Figure 7(b). The formulation of the physical quantities are provided in the rest of this section. Let us make an assumption of a fixed conversion gain for a pixel. And, let's look at the signal to noise ratio (*SNR*) versus photo-diode area. In

order to explain the *SNR* better, the analysis is done in terms of charge. The signal level can be described as a function of area as

$$Q_{signal} = K_1 A. \quad (11)$$

The major noise source inside the pixel include the following: the kTC noise from the reset path, the dark current noise from the diode leakage and the shot noise from the diode due to the unstable electron fluctuation of the diode. The equations for these three terms can be formulated as

$$Q_{kTC} = \sqrt{kTC_{pix}} = K_2\sqrt{A}. \quad (12)$$

The kTC noise is a time independent noise therefore it is can considered a constant noise floor. The dark current noise can be considered from two sources: the edge diode and the area diode.

$$Q_{dark} = K_3\sqrt{A} + K_4 A, \quad (13)$$

where K_3 and K_4 are coefficients of the dark current for the edge component and the area components. According to the experiments from previous test slots [10], the edge component is the dominating factorize the dark current. This dark current noise is a time-dependent noise. Therefore, for longer integration time, the total dark electron increase. The photon shot noise is a signal dependent and, thus, a time dependent noise. It can be formulated as

$$Q_{shot} = \sqrt{N_{signal}q} = \sqrt{Q_{signal}q} = K_5\sqrt{A}. \quad (14)$$

Other noise sources such as source follower fixed pattern noise (FPN), 1/f noise, and MOSFET thermal noise are not directly related to the pixel photo-sensitive area. Therefore, the first order signal to noise ratio equation can be written as

$$\frac{S}{N} \cong \frac{K_1 A}{K_2\sqrt{A} + K_3\sqrt{A} + K_5\sqrt{A}} \propto \sqrt{A} \quad , \quad (15)$$

where area component for the dark current is considered to be dominated by the edge leakage current. Therefore, the *SNR* model of a pixel indicates that larger photo-element size will provide better signal to noise ratio and, in fact, the growth is in square root sense. That means the *SNR* grows with the pixel pitch. Therefore, in order to maintain good SNR at small pixel size, increasing fill factor is essential.

If a bulk-diode is used as the photo-sensitive element and this element is assumed to have a fixed pixel area of 9 μm X 9 μm, then the fill factor of the various pixel structure with different transistor counts is shown in Figure 8. This clearly shows that number of transistor will serve as the fundamental limitation for pixel miniaturization. Technology scaling can help to relax the design constraint and, however, two transistor and one transistor pixels are important if the pixel is considered to be scaled down to be below 5.0 μm pixel pitch.

6. EXPERIMENTAL RESULTS

As shown in Figure 9, the threshold voltage of the high threshold voltage transistor on 13 test structures are measured. For each test structure, there are 24 devices. The measured results are centered around two controlled values (1.2 volt and 0.9 volt). The consistency of the threshold voltage is high for the HP's 0.35 μm CMOS technology. For the prototype chip, a designed threshold voltage 1.2 volt is used.

The die photo of the prototype chip is shown in Figure 10. In the center, the green area is the pixel array. The row decoder, column decoder and the column level signal buffer is covered by the metal 4 photo mask to prevent the parasitic photo-electric effects. The output response of a single salient integration mode pixel is shown in Figure 11. The clock period used to this measurement is 30 ns. This means the whole whole row access can be completed in 90 ns. In Figure 12, the output response of a readout channel is measured. The clock period used in this measurement is 50 ns. The whole column access can be completed in 150 ns. With such a performance, a 2 Mega pixel array (1600X1200) can be read out within 300 msec if only one single channel is used. The power consumption of the readout circuit with the pre-designed threshold voltage of 1.2 volt is obtained. 30 frame/sec is used. 5.0 mW is measured for 3.3 volt power supply. and 0.85 mW is measured for 2.0volt supply.

7. CONCLUSIONS

A scalable CMOS image sensor design for low voltage and low power applications is presented. It includes a salient integration mode pixel design and a low voltage low power mixed-signal readout architecture. The salient integration mode operation can be applied to a two transistor pixel design or a one transistor pixel design. Such pixel miniaturization is the enabling technology for high resolution imaging. The proposed low voltage low power readout architecture is very effective in reducing the frame readout time. In combination, it is a highly cost effective solution to future low cost and low power imaging.

8. ACKNOWLEDGEMENTS

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9. REFERENCES

[1] S. K. Mendis et al., "CMOS active pixel image sensors for highly integrated imaging systems," *IEEE JSSC*, vol 32, no. 2, pp. 187-197, Feb. 1997.

[2] E. R. Fossum, "Architecture for focal-plane image processing," *Optical Engineering*, vol. 28, no. 8, pp. 865-871, Aug. 1989.

[3] A. M. Chiang et al., "A high speed digitally programmable CCD traversal filter," *IEEE JSSC*, vol. 18, no. 9, pp. 745-13, Sept. 1983.

[4] E. R. Fossum et al., "Active pixel sensor with intral pixel charge transfer," US patent 5,276,407, 1994.

[5] P. B. Denyer, "Matrix array imager sensor chip," US patent 5,345,266, 1994.

[6] B. Fowler et al., "CMOS image sensor with pixel level A/D conversion," US patent 5,461,425, 1995.
[7] T. Kuroda et al., "A 1/4 inch 330k square pixel progressive-scan IT-CCD image sensor with sub micrometer channel width," *ISSCC*, pp. 184-185, Feb. 1996.
[8] M. Furumiya et al., "A 30 frame/s 2/3 inch 1.3M pixel progressive scan IT-CCD image sensor," *ISSCC*, pp. 188-189, Feb. 1997.
[9] R. H. Nixon et al., "128x128 CMOS photodiode type active pixel sensor with on-chip timing, control and signal chain electronics," *Proc. SPIE, vol. 2415, Charge-Coupled Devices and Solid-State Optical Sensors V, paper 34, 1995.*
[10] S. Mendis et al., "Active Pixel Image Sensors in 0.35 CMOS Technology", Proc. IEEE Workshop on Charge-Coupled Devices & Advanced Image Sensor, Bruges, Belgium, Jun. 1997.

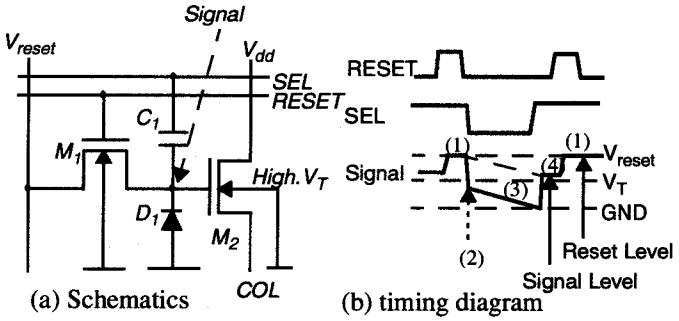


Figure1: Circuit schematics and timing for 2T CMOS imaging pixel.

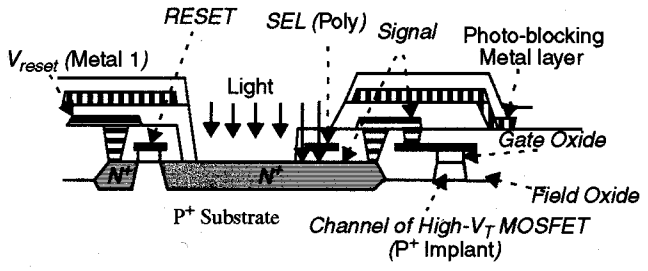


Figure 2: Cross-section diagram for a salient integration-mode pixel.

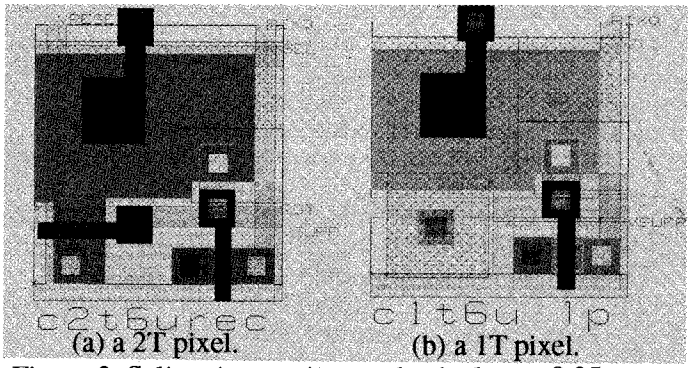


Figure 3: Salient integration mode pixels at a 0.35 μm CMOS technology.

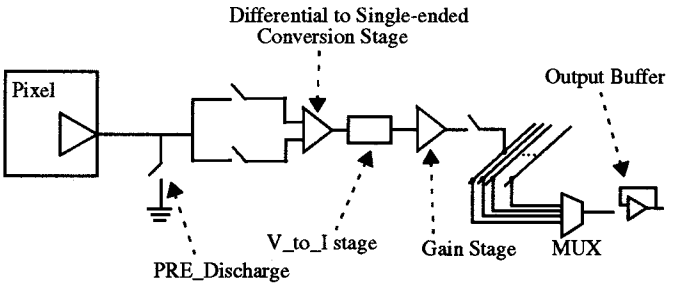


Figure 4: Block diagram for the low voltage low power readout channel.

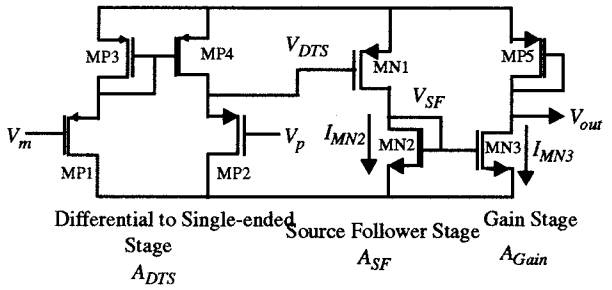


Figure 5: Circuit Schematic for the Gain Assisted DTS Circuit.

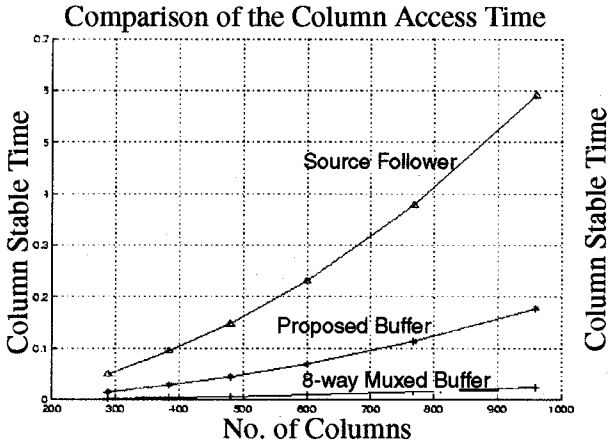
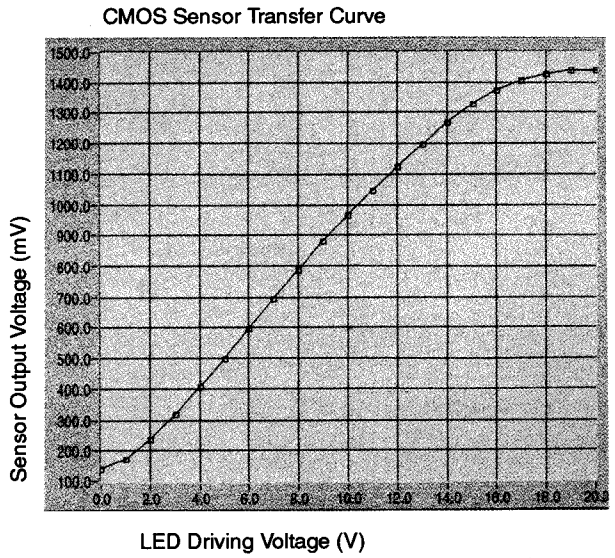
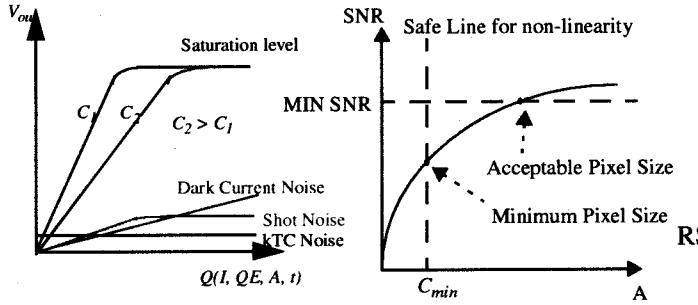


Figure 6: Total column access time per frame versus number of column.



(a) measured result.



(b) analytical model. (c) Oixel design rule.

Figure 7: Relationship of the signal level and the noise floor.

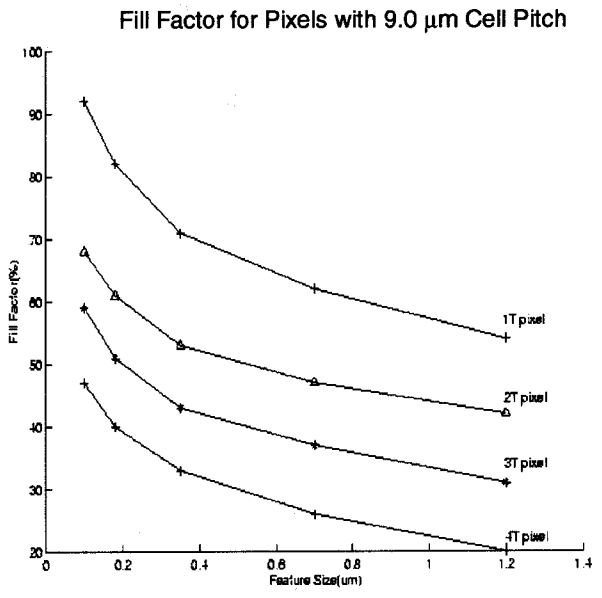


Figure 8: Fill factor versus technology scaling for a fixed pixel size.

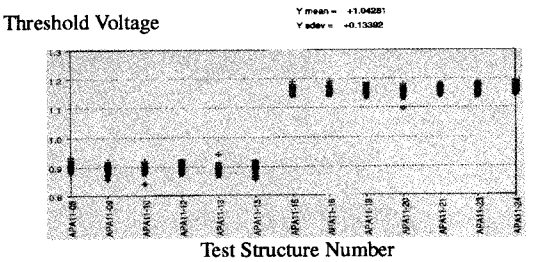


Figure 9: Measurement for the threshold voltage for the high V_T device on various test structures.

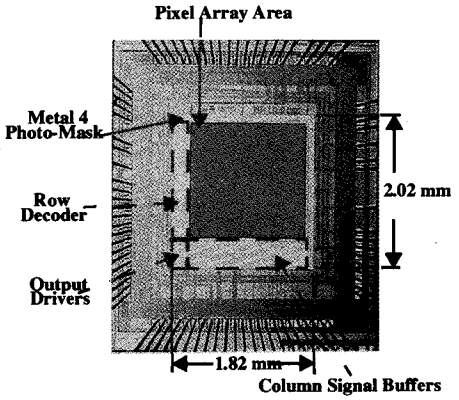


Figure 10: Die photo of the prototype chip with 256 X 256 2T pixels.

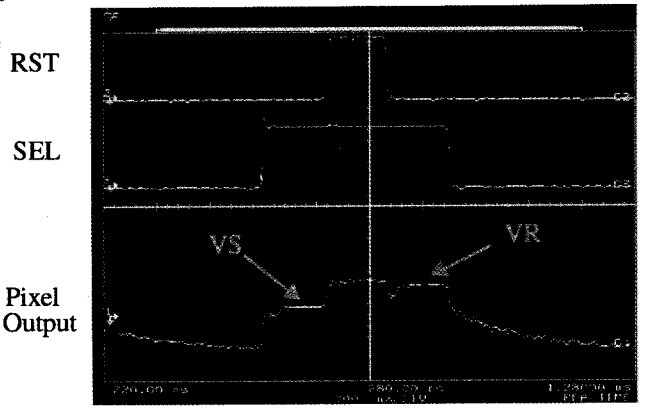


Figure 11: Measured pixel output response by HP 54542C digital oscilloscope.

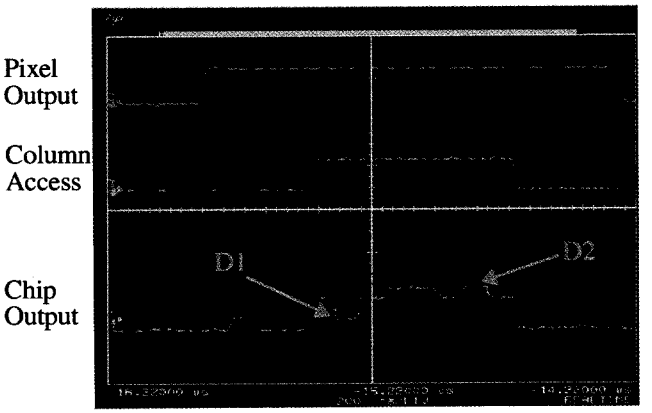


Figure 12: Measured sensor chip output response by HP 54542C digital oscilloscope.