Networked CAD Systems

Session Chair: Giovanni De Micheli, Stanford University, Stanford, CA, USA

Panellists: David Ku, Escalade Inc.
Luca Benini, Stanford University, Stanford, CA, USA
David Lidsky, U.C. Berkeley, Berkeley, CA, USA

Computer-aided design (CAD) tools have become an essential part in the design flow of any complex electronic system. At the same time, the number of tools needed to implement complex systems is increasing and such tools are generally provided by several suppliers. Integration of CAD tools into unified frameworks prompts for an increasing effort in the creation of standard interfaces. The definition of standard formats for design descriptions such as VHDL and EDIF has been an important milestone in this direction. However, the user interfaces provided by different CAD vendors still lack in uniformity and compatibility.

Moreover design teams are often geographically dispersed, even though they may be working on different parts or facets of the same design. Design reuse of libraries, hard/soft macros, and embedded software may require access to resources that are also geographically dispersed. Fortunately, computer networks such as *intranets* and the *internet* provide pervasive reliable links among designers and design data, as well as an useful means of storing and classifying information. In addition, network browsers and helpers have simplified the access to remote and distributed information, by providing a uniform mechanism which is easy to learn.

The use of computer-aided design tools over intranets and the internet is raising a large interest because of research and business opportunities. Most corporations, where designs are performed at different sites, use intranets for data sharing and communication. Computationally demanding tasks can be performed on high-performance servers remotely connected to the designers by intranet links. Nevertheless, CAD tools are still developed and marketed to be used in specific locations, and the use of intranets to improve upon the design cycle is left to the needs and the ingenuity of the designers.

We expect to see distributed CAD environments for intranets on the market soon. Such environments will make transparent to the designer the location of tools, libraries and design data. This will increase designers' productivity by providing them with uniform access to resources as well as faster response time on computationally-expensive tasks because of load balancing across the network.

The next challenge is to develop distributed CAD environments over the internet. The *world-wide web* (WWW) provides a link to virtually all users of scientific computing and WWW browsers provide *de facto* standard user interfaces. Whereas the WWW has been mainly used until now for information retrieval, a large potential lays in its use for distributed information processing and in leveraging network programming tools.

CAD programs and environments on the WWW can be developed for scientific and/or commercial reasons. The WWW is an ideal means for dissemination of information. Thus, CAD tools developed in academia may be interfaced to the WWW for the purpose of supporting remote access and demonstrations, and providing world-wide exposure. Collaborative research programs at different institutions can use the WWW as a way of interfacing CAD tools. In this perspective, the WWW may play a role similar to the original role of ARPANET.

The commercial opportunities for distributed CAD services are promising as well. New tool usage paradigms may emerge. Designers could temporarily connect to a tool provider, perform a specific task and be billed on a usage-time basis. Design flows may incorporate the use of remotely-located tools, with different costs and objectives, and customizable according to the design goals. CAD vendors may offer free, or limited-cost, tool usage to advertise their products.

ED&TC '97 on CD-ROM

There are clearly many ways of envisioning the development of networked CAD systems on intranets and on the internet. Difficulties may arise due to several factors, including data consistency, network loads, limited bandwidth and response delays. Design of electronic products using the internet must address security problem related to design and technology data. Despite these difficulties, the rapid growth of network-based products and the potential payoffs of networked CAD make this field an exciting area of research.

Multichip Packages for Consumer Applications

Session Chair: Math Muris, Philips Research/ED&T, The Netherlands

Panellists: Herman Casier, Alcatel Mietec, Brussels, Belgium
Urs Fawer, Philips Semiconductors, Zurich, Switzerland
Wolfgang Radlik, Siemens Research, Munich, Germany
Claudio Truzzi, IMEC, Leuven, Belgium

Application of Multichip Packages is becoming more and more interesting for small-sized, light-weight, cost-sensitive portable consumer equipment. After hearing our panellists on marketing, design, testing, substrates, packages, ppm budgets and KGD issues related to MCPs for consumer applications, we like you to join us in a discussion on the pros and cons of this technology.

Since the dark ages of mainframe computers, Multichip Modules have been used for achieving performance targets which couldn't be met with existing Printed Circuit Board technologies. The high costs for design, manufacturing and test of these Multichip Modules were acceptable for professional applications.

Our bright current age, full of portable multimedia consumer applications, also cries out for Multichip Modules, but now the driving forces are small-sizes, light-weight, low power, combination of technologies, time-to-market and low costs.

Our panelists will introduce you to the issues involved with design, technology, manufacturing and test of Multichip Packages for consumer applications.

Wolfing Readily will give an overview of the current status of substrates and packages for MCPs, with a focus on consumer applications.

Cloud Truss will present MCM-specific design issues concentrating around availability and infrastructure, it's impact on the early stages of design and what strategies are being applied in the US and in Europe to address these issues.

Math Moors will summarize test strategies for obtaining KGDs and MCPs based on underlying requirements for quality and reliability, geared towards cost sensitive consumer products.

Urs Fawer will concentrate on design experiences (constraints from sub-contractor/customer, lead time, "design-flow"), examples and ad-hoc solutions.

Herman Casier will take the position that MCPs will only provide a temporary solution, because high volume demands will always lead to a dedicated IC technology, resulting in a single die solution.

Following these introductions, the audience is invited to discuss with the panel the pros and cons of this MCP technology.

Deep Submicron CAD

Session Chair: Ralph Otten, Delft University of Technology, Delft, The Netherlands

Panellists: Keith Baker, Philips Research, Eindhoven, The Netherlands
Raul Camposano, Synopsys Inc., Mountain View, CA USA
Antun Domic, Cadence Design Systems Inc., San Jose, CA, USA
Patrick Groeneveld, Compass Design Automation, San Jose, CA, USA

As microstrip features scale into regimes of close to or below a tenth of a micron new metrics obtain importance beside the traditional area, time and power objectives.
A decade of analysis has shown the increasing effect that interconnect is going to have,
as VLSI systems are effectively transformed into microwave circuits of unprecedented complexity. Not only delay requires a totally new approach, future design systems have to be able to prevent detriments caused by crosstalk and resistive voltage drop in an essentially three-dimensional configuration.

The return on investment of the new technologies will be very disappointing when these effects can only be controlled by large safety margins.
This implies that noise immunity is going to be one of the new metrics to enter the field and will extort compromises with timing and area demands.

Also, whatever the solutions are going to be, how will they affect the robustness of layout, and finally, how do we find out efficiently whether the circuit should pass the test stages.

It is clear to everybody that the interplay of different stages in design is going to become more intensive, even so that no longer layout design, logic synthesis and higher levels of synthesis can be treated sequentially or even iteratively. A complete integration into what already has been coined the design planning approach will be mandatory.

The questions that are going to be tackled in this session are:

- How are the new metrics going to be incorporated into the tools for designing these so-called deep-submicron circuits?
- How is one to retain the relative design comfort of the digital abstraction?
- What are the test methodologies going to be like for this new generation of VLSI circuits?
- How are the upto now separate design stages to be integrated in the design plan?
- Will vendors be capable to develop the right tools far from where technology is being developed, or is this going to be the exclusive terrain of corporate CAD?
- And is university research going to have a place in it after it had such a significant contribution to the development of analysis for three-dimensional deep submicron structures?