The Input Pattern Fault Model and Its Application

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Faults in circuits are typically represented by the single stuck-line (SSL) model, which allows any gate input or output line to be permanently fixed or stuck-at a logical 0 or 1. A deficiency of the SSL model is that it does not accurately reflect all the defect types of current IC technologies. For example, CMOS defects that cause the unintended connection (short) of signal lines cannot be directly modeled as an SSL fault, and are not always detected by test patterns aimed at SSL faults. More recent work [1] has shown that arbitrary changes in standard cell functions due to spot defects are quite possible. Hence, fault models that can directly analyze such functional faults seem likely to grow in importance.

The *input pattern* (IP) fault model is a functional fault model that allows for both complete and partial functional verification of every circuit primitive, independent of the design level. Here, we formalize the model and provide a method for analyzing IP faults using SSL-based tools.

A fault f_j can change a module's response to an input pattern ip_k from v_k to v_k'; we denote this change in functionality by $ip_k \rightarrow (v_k , v_k')$ and refer to it as a *single input pattern* fault, or simply as an IP fault. The pair of distinct values (v_k , v_k') denoting the good and faulty output patterns is the *error* corresponding to the fault. The IP fault model allows a single module to be affected by a set of IP faults (a *multiple IP fault*) $F = \{f_1, f_2, \ldots, f_k\}$. For example, the change in the 2-bit AND gate function to an XOR is equivalent to $F = \{01 \rightarrow (0,1), \rightarrow 10\ (0,1)\}$.

Figure 1 shows a gate-level implementation of a 2-bit AND function that has a subset of SSL faults equivalent to all the possible IP faults of the AND function. Similar circuits exist for an arbitrary *n*-input, *m*-output function. The ISCAS85 circuits were transformed by replacing all gates *C* (with up to four inputs) with equivalent circuits *C** similar to those of Fig. 1. SSL-based ATPG and fault simulation tools were applied to the transformed ISCAS85 circuits to obtain the results in Table 1. Our experiments show that IP tests tend to detect non-targeted faults. For transistor stuck-on (TSO) and bridging faults, high fault coverage was achieved for the benchmarks, and in the case of TSO faults, was achieved using fewer tests than those generated specifically for detecting these faults.

We have also generated IP test patterns for gate- and register-level designs of a carry-lookahead adder adapted from [2]. The gate-level design is completely testable for all IP faults, but redundant IP faults at the register-level do exist. The redundant IP faults map to don't care entries in the truth tables of the adder's modules which essentially correspond to the *permissible functions* [3] of the design. This type of redundancy has been exploited to enhance the testability of large carry-lookahead adders and ALUs [4, 5]. Large amounts of IP redundancy also have been found to exist in the irredundant versions of the ISCAS85 benchmarks. Current work is studying ways to effiiciently exploit IP fault redundancy to enhance testability and reduce circuit size.

We have formally characterized IP faults as a general method for modeling the faulty behavior of IC's. The relationship between SSL and IP faults has been used to generate IP tests using standard SSL-based tools. The resulting IP tests do well in detecting other types of faults.

IP fault	SSL fault
$00 \rightarrow (0, 1)$	$a/1$
$01 \rightarrow (0, 1)$	$c/1$
$10 \rightarrow (0, 1)$	$b/1$
$11 \rightarrow (1, 0)$	$d/0$

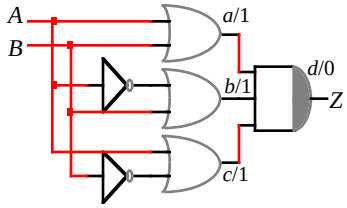

Figure 1: Equivalent SSL and IP faults in a 2-level implementation of the two-bit AND function.

	SSL tests	TSO tests	I_{ddq} tests	Bridge tests	IP tests
No. of tests	95	368	25	53	147
SSL coverage	100%	–	–	–	100%
IP coverage	95.7%	–	–	–	100%
TSO coverage	–	98.0%	–	–	98.2%
I_{ddq} coverage	–	–	100%	–	100%
Bridge coverage	–	–	–	94.4%	95.4%

Table 1: Average fault coverage for the ISCAS85 circuits by IP tests and other fault-specific tests.

References

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