Design of Partially Paralle Scan Chain

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Abstract

This paper presents a design-for-testability technique, called partially parallel scan chain (PPSC), which aims at reduction of test length for sequential circuits. Since the partially parallel scan chain allows to control and observe subset of flip-flops (FFs) concurrently during scan shift operations, the number of scan shift clocks is reduced.

1. Introduction

In PPSC, some FFs are arranged in parallel and some FFs are in serial. Since the FFs arranged in parallel can be controlled and observed concurrently, the number of scan shift clocks is reduced. Although a subset of states can not be set by scan shift operations, the proposed method can detect all the sequentially detectable faults. PPSC requires only one scan input line and one scan output line, thus it is different from parallel scan methods[1]. Moreover PPSC reuses the original function for its construction as much as possible.

2. Configuration of PPSC

Parallel FFs in PPSC are found in particular subcircuits. In this paper, four types of subcircuit are presented and the configurations of PPSC are described related to the subcircuits. In Fig.1, the thin solid lines denote an original subcircuit, and the thick solid lines from d_{in} to d_{out} denote a part of PPSC. Either normal data x or scan data d_{in} is selected by MUX and set to FFs. Variable mc denotes a mode control signal. When mc = 0 the circuit behaves normal operation, and when mc = 1, it behaves scan shift operation.

[Type-1] The FFs driven by the same fan-out stem can be arranged in parallel as shown in Fig. 1(a). The two FFs can be concurrently controlled. In this PPSC state (α_1,..., α_k) = (0,..., 0) and (1,..., 1) can be set and only FF α_1 can be observed. Faults which require the other states are sequentially undetectable.

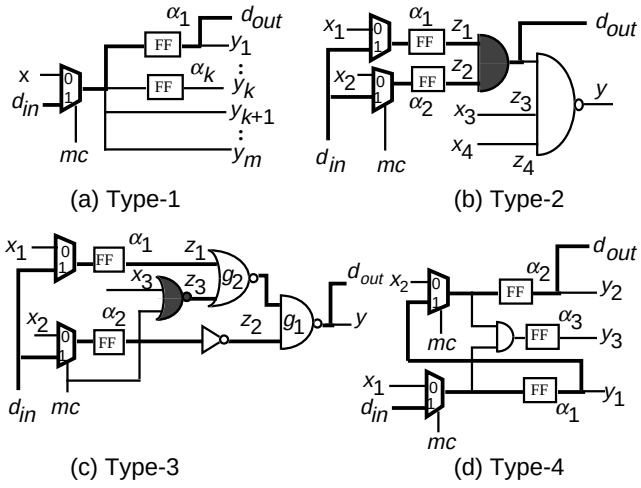

Fig. 1 Configuration of PPSC

[Type-2] When some FFs drive a same gate, these FFs can be arranged in parallel as shown in Fig. 1(b). Note that the black filled gate is added to observe the two FFs concurrently. The faults which require state (0, 1) or (1, 0) for their detections are sequentially undetectable except for faults on z_1 and z_2. Stuck-at one fault on z_1 and z_2 can be tested as follows. First, an input vector applied so that state (0, 1) or (1, 0) is set. Next, scan shift operation is performed. Then the fault is activated and its effect is scanned out.

[Type-3] In subcircuit of Fig.1(c), gate g_1 and g_2 can be united into one gate by De Morgan's law and the associative law. The FFs in such a subcircuit can be arranged in parallel. The black filled gate is added in order to make the signals of z_3 inactive during scan shift operations.

[Type-4] When there are three FFs which are driven by the two lines x_1 and x_2, PPSC is configured as shown by thick solid lines in Fig. 1(d). In this subcircuit, FF α_3 is not necessary to be independently controlled and observed.

3. Experimental result

We experimented for ISCAS '89 benchmark circuits. Table 1 shows the results. The test length is calculated by

$$L = n (v + 1) + v \qquad (1),$$

where n is the number of scan shift clocks or FFs and v is the number of test vectors. Columns "serial" show the results of case that all FFs are arranged in serial. Columns "PPSC" show the results of the proposed method. It is found that PPSC achieves short test lengths.

Reference

[1] S. Narayanan, R. Gupta and M. Breuer, "Configuring Multiple Scan Chains for Minimum Test Time," Proc. Int'l Conf. on CAD, pp. 4-8, Nov. 1992.

Table 1 Experimental results

	serial			PPSC			
circuit	FF	test vector	test length	scan shift clock	test vector	test length	ratio
s5378	179	111	20159	153	114	17709	0.878
s9234	228	148	34120	199	153	30799	0.903
s13207	669	243	163479	506	236	120158	0.735
s15850	597	125	74347	580	128	74948	0.995
s38417	1636	141	232453	1584	137	218729	0.941

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