A Scheme For Multiple On-chip Signature Checking For Embedded SRAMs

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Introduction : Pseudorandom self testing of embedded memories is commonly used because of its simplicity [1]. A novel scheme pseudorandom testing with multiple on-chip signature checking ($MOSC$) has been proposed in [2]. Although this scheme results in significant reductions in aliasing probability at no significant increase in area in most cases, the test area and time overhead may be excessive if the circuit contains multiple embedded RAMs of various sizes. Example of such circuits are the ASICs for the telecommunications. In this paper, we propose a Static-RAM BIST scheme, based on the $MOSC$ scheme, which is applicable for testing chips that have multiple embedded RAMs of various sizes.

Basic Idea : Our scheme is based on the observation that when two memories are identical, the following advantages exist in terms of testing these memories: (a) there is a 50% saving in the size of the test controller area (b) the same test pattern generator and address generator can be shared by the two memories (c) there is a 50% saving in the fault simulation effort.

If the circuit contains memories with different widths, we atempt to partition them into segments of identical widths. If there are memories with different lengths, we synchronize their test cycles, so that the same test patterns can be used to test all the memories.

Beside, the reduction in aliasing probability and the test area overhead, the proposed transformations make it easier to carry the exact fault simulation, since in this case it is enough to perform fault simulation for a single memory alone.

Results : Table 1 shows the area occupied by the test controller for the proposed scheme for several ASIC telecommunication chips [1], using 1 μm CMOS technology. The percentage of the saving in the area resulting from partitioning alone (P), synchronizing alone (S), or both compared to that without the optimization techniques for 10, 20, and 30 check points, resp. A saving of up to 80% can be obtained for some chips with large number of embedded RAMs. In some cases e.g. the $AENT$ chip [1], though the partitioning alone is not applicable, incorporating this technique with the test synchronizing will significantly improve the area overhead.

Table 1: Test controller area.

Chip	Embedded Memories	Area (μm^2)	% *Area saving*		
			P	S	$P\&S$
$AELT$	$38 \times 8, 16 \times 30$	155,350	15	46	76
	$143 \times 32, 26 \times 32$	294,250	16	49	80
	$16 \times 32, 208 \times 32$	433,150	16	50	81
$AENT$	130×6	147,000	–	37	72
	$208 \times 8, 230 \times 8$	275,750	–	39	76
	$64 \times 8, 676 \times 32$	404,500	–	40	78
$Chip_3$	512×5	64,400	39	–	39
	512×10	112,000	44	–	44
		159,600	46	–	46
$Chip_4$	$2 \times (64 \times 8)$	164,050	61	61	76
	$2 \times (512 \times 8)$	310,750	64	64	80
	$2 \times (512 \times 16)$	457,450	65	65	81

References

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