SISSSI – a tool for dynamic electro-thermal simulation of analog VLSI cells

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With the decreasing feature sizes and increasing packaging densities thermal effects influence more and more the operation of integrated circuits. The accurate consideration of thermal effects while predicting the electrical behaviour of the ICs became crucial in case of high performance integrated circuits both for analog and digital ones.

The SISSSI electro-thermal simulator family can be applied for the above purpose, both for analog and digital designs. The common feature of the SISSSI versions (SISSSI-*Classic* and SISSSI-*Logitherm*) is that they construct the layout based thermal model of the IC automatically and consider accurately the effect of the chip encapsulation as well.

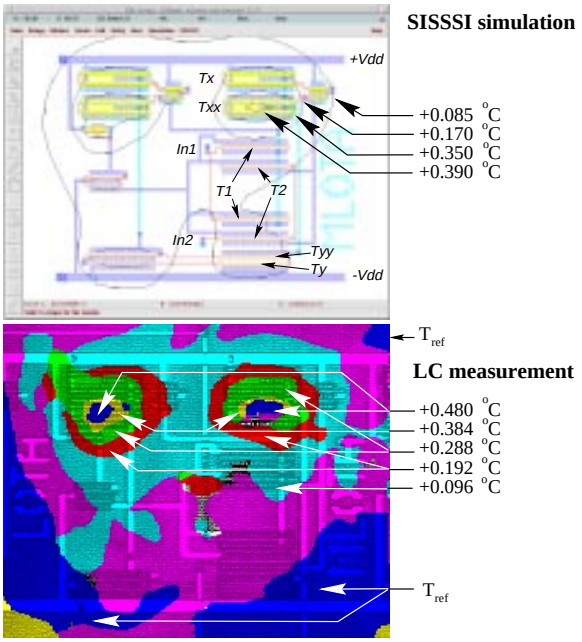

Figure 1: Steady-state results of a CMOS transconductance operational amplifier.

SISSSI-*Classic* is aimed at device level (analog) electro-thermal simulation, while SISSSI-*Logitherm* can be used for the cell (gate) level logi-thermal simulation of digital designs [1]. Here we present only the developments in the SISSSI-*Classic* version [2], [3]. Its main features are the following: Application of the method of *simultaneous iteration*, automatic electro-thermal netlist extraction from the layout, efficient compact thermal modeling of the IC based on its simulated dynamic thermal behaviour with the application of the NID technique (network identification by deconvolution) [4], considering the thermal effect of the chip encapsulation, electro-thermal modeling of all types of semiconductor elements, consideration of the Seebeck-effect taking place at *Si-Al* and *poly-Al* contacts. With these features electro-thermal DC, AC, and transient simulations are possible.

Simulation results obtained by SISSSI-*Classic* compared with measurements are presented in the figures.. As it can be seen on the figures, there is a perfect agreement between the simulation and measurement results.

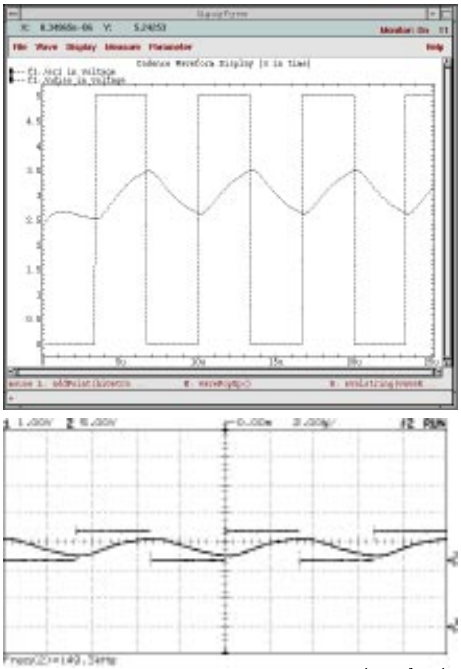

Figure 2: Electro-thermal transient simulation and measurement results of a thermal delay line.

References

[1] V. Székely et al. In *Proc. of the 2nd THERMINIC Workshop*, pp 79–88, Budapest, Hungary, 1996.

[2] V. Székely et al. Self-consistent electro-thermal simulation: fundamentals and practice. *Microelectronics Journal*, 27:(under publishing), 1996.

[3] V. Székely et al. In *Proc. of ED&TC'96*, p. 604, 1996.

[4] V. Székely. In *Proc. of the 2nd THERMINIC Workshop*, pp 21–26, Budapest, Hungary, 1996.

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