Test Synthesis for DC Test of Switched–Capacitors Circuits

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Built–In Self Test (BIST) consists of integrating totally or partially a Test Pattern Generator (TPG) and/or a Response Analyzer (RA) in the same chip with the Circuit Under Test (CUT). Generally, an efficient analog test requires the monitoring of several performances by applying different frequencies as test stimuli. For BIST application, the integration of a frequency TPG and RA can not be economically viable for most applications because of their corresponding area overhead and complexity. BIST techniques based on frequency analysis are very expensive for the silicon area. On the other hand, BIST solutions based on a DC test remain poor concerning the fault coverage. This is true if no Design For Testability (DFT) elements are used in conjunction with a DC BIST to eliminate this problem. Exactly, our approach consists of using some DFT means so as all defects of SC circuits become detectable in the DC domain. Then a DC stimulus as an existing voltage source Vdd, Gnd and Vss corresponds to a simple TPG while the RA is a small window comparator. Finally, the addition of these DFT elements allows to decrease considerably the DC BIST hardware and corresponds in fact to a tradeoff between BIST complexity and DFT resources. With this mixed BIST/DFT technique we obtain a comparable fault coverage than frequency based approaches and this for a lower hardware cost.

With our DFT transformation technique any SC circuit becomes a cascade of voltage amplifiers in which all the capacitors are represented in simple ratio forms. As a simple example, let us consider a typical SC low–pass filter of transfer function $H(z) = \frac{C1z^{-1}}{C3 + C2(1-z^{-1})}$. Without DFT, the optimal test of this circuit requires two frequencies. Our methodology, illustrated in figure 1, consists of adding four switches so as the capacitor C2 becomes switched (P.T) in the test mode (T=1) and non–switched (I+$\overline{T}$) in the normal operating mode. In the DC domain (z=1), the filter becomes a voltage amplifier that has a gain of $H(1)_{[T=0]} = \frac{C1}{C3}$ in the normal mode that is with T=0; this corresponds to the first previous test frequency. Of course, with T=0 the switched–capacitor C2 has exactly the same behavior than in the original schema. Now, since C2 is switched (I+$\overline{T}$, P.T) in the test mode T=1, and C3 is no longer switched (I+T, P.$\overline{T}$), the new transfer function is then $H(z)_{[T=1]} = \frac{C1z^{-1}}{C3\ (1-z^{-1}) + C2}$. In this test configuration and with a DC stimulus (z=1), the filter becomes a new voltage amplifier with a DC gain equals to $H(1)_{[T=1]} = \frac{C1}{C2}$. With these two configurations, T=0 and T=1, the DC gain has a sensitivity equals to one for each of the capacitors. However, an extra digital block is needed for the control signals (I+T, I+$\overline{T}$, P.T, P.T).

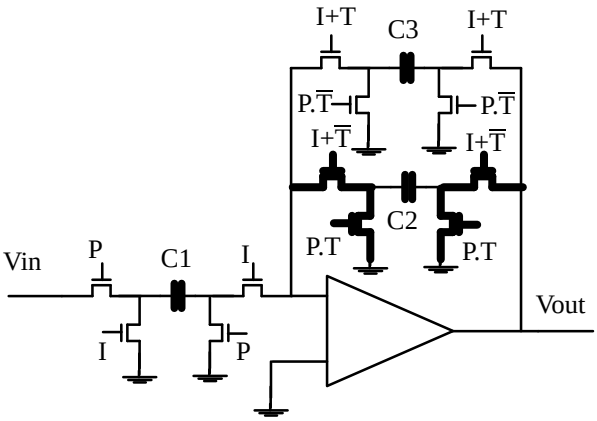

Figure 1 : Modified SC low–pass filter

In conclusion, this abstract presents a test technique for SC circuits, not limited to SC filters, that re–configures the circuit so as it realizes a cascade of DC voltage amplifiers. The reconfiguration corresponds to the addition of some extra switches in the large signal path and all components are sensitive to a DC stimulus. Parametric faults and components mismatches which are crucial in analog circuits are then detectable in the DC domain. Starting from the fluency graph description of a SC circuit, a high level test synthesis algorithm has been also investigated. It allows to automatize in a more formal way this DC test technique. Simulations of the performances degradation of a SC biquadratic filter have validated the suitability of the approach.

[1] C. Dufaza and H. Ihs, "Design for DC Built–In Self Test and Partial Diagnosis of Switched–Capacitor Circuits", 2nd Int. Mixed Signal Test Wkshp., Quebec, May 1996.

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