

An Asynchronous Architecture For Digital Signal Processors

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Abstract

We propose an asynchronous[1] architecture for digital signal processors. This is based on a modification of the counterflow pipeline[2]. In addition to registers, we apply the counterflow technique to memory operands as well. This results in an asynchronous architecture with good performance potential for DSP. We describe the architecture below.

1 Counterflow

We propose a modification to the counterflow pipeline [2], which has several interesting properties useful for DSP. Operations in our pipeline can have memory or register operands and targets. We associate each memory operand or result with a hash code. These codes, distinguished from register codes by a special prefix, are placed in the operand or result ID fields as the register codes are. This extension is useful for DSP algorithms where computations depend on immediately preceding computations and operands usually are from memory.

2 The Architecture

The architecture we propose will have the following parts:

- A fetch, pre-decode and discontinuity management unit, which decodes branches, calls, etc early and handles modifying the fetch counter,
- an operand request unit, which also generates tags for memory operands,
- an assemble unit, which puts the instruction and operands in the right form for the pipeline,
- a register file unit, with one write port and two read ports, a memory interface,
- a modified counterflow pipeline unit,
- a scoreboard management unit,

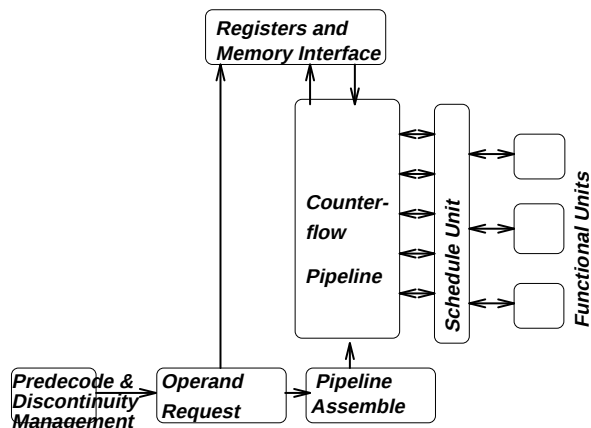


Figure 1: Proposed Architecture

and multiple Functional units.

3 Future Work

Initial architectural simulation in VHDL has been encouraging.

We plan to do a fairly detailed design of such a processor to verify that it is indeed possible to achieve good results with the asynchronous approach and to examine lower-level design issues.

References

- [1] Scott Hauck. Asynchronous design methodologies: An overview. *Proceedings of the IEEE*, 83(1), January 1995.
- [2] Robert F. Sproull, Ivan E. Sutherland, and Charles E. Molnar. The counterflow pipeline processor architecture. *IEEE Design & Test of Computers*, 11(3):48–59, Fall 1994.