

Full Custom Chip Set for High Speed Serial Communications up to 2.48Gbit/s

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Abstract

A full custom chip set has been developed (within the ESPRIT III SPIBOC project) to perform high speed serial-parallel conversion on an optical link. It is composed by two complementary circuits for 8-bit parallel to serial multiplexing and serial to parallel demultiplexing (@2.5 Gbit/s). Each integrated circuit has four identical modules in order to optimize area on board. An aggregated bit rate of 10Gb/s is achieved

The purpose of the multiplexer chip, called HSS (High Speed Serialiser), is to adapt incoming data from external circuits to the laser driver required to transmit the information to the optical/electrical interface. In a similar way, the demultiplexer chip, called HSD (High Speed Deserialiser), takes the serial flow of transmitted data from the receiver and converts it to the primary 8-bit-wide parallel format.

Every data and clock signals conforms to the LVDS standard (Low Voltage Differential Signals for Scalable Coherent Interface). The circuits can also work together with ECL and bipolar CML levels

The high speed input clock is a 1.24 GHz clock. It is internally doubled in the chips in order to obtain the 2.48 GHz clock; in this way, the 1.24 GHz clock can be

transmitted to the far-end using the same kind of optical fiber as the one used for the data. Due to the lack of standard layout libraries working at the high speed needed for these ICs, a basic library of full custom gates has been developed using the HSB2 (high speed bipolar) technology from SGS-Thomson. It contains over 60 different cells, including several layout version for each cell, depending on the layout and speed requirements. The basic architecture for the cells was CML.

The global layout was full-custom made.

Both integrated circuits are built with the same size and pin count. The inputs and outputs were placed symmetrically in order to improve the routing to the interfaces at the board level.

The ASICs characteristics are:

- Area: 5.13 x 7.15 mm each.
- Pin count: 180 pins (100 signal pins and 80 power pins).
- Power consumption: 3.8 watts for HSS and 4.1 watts for HSD.
- Differential I/Os. Compatible with LVDS

In figures 1 & 2 photographs of the chips are shown.

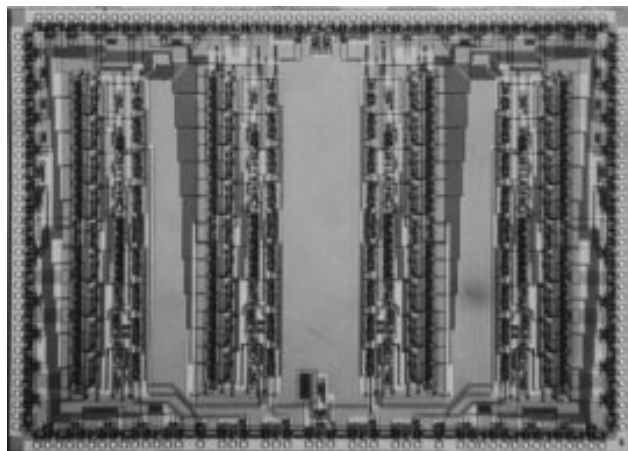


Figure 1: HSS photograph

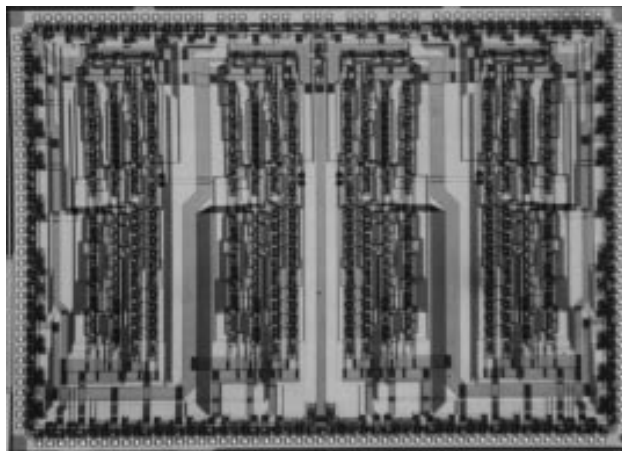


Figure 2: HSD photograph