

A New Field Programmable System-on-a-chip for Mixed Signal Integration

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Abstract

A new RAM-based, mixed-signal, multicontext dynamically reconfigurable Field Programmable Device with on-chip microprocessor is described. A completely integrated mixed-signal CAD and microprocessor programming environment is used to design and simulate electronic systems composed by microprocessor code and digital and analog hardware. The very flexible communication between the microprocessor, the configurable digital cells and the programmable analog blocks makes possible powerful integration, real-time emulation (internal signals and configuration are available to the microprocessor) and advanced run-time reconfiguration.

As the complexity of electronic systems grows, it becomes more and more difficult to follow a traditional design methodology of working separately on different subsystems with different design and prototyping tools. Typically, these systems may include a digital part, an analog part and a software program running on a microprocessor or microcontroller. However, these three domains (digital, analog and software) have to be designed and prototyped separately, using different CAD tools and hardware parts for each one.

Within this framework we introduce the FIPSOC (Field Programmable System On Chip) prototyping and integration system, consisting of a mixed-signal Field Programmable Device (FPD) with a standard microprocessor core (a 8051), a suitable set of CAD tools to easily program it, and a set of library macros and cells which support a number of typical applications to be easily mapped onto the FPD and migrated to an ASIC afterwards, if required.

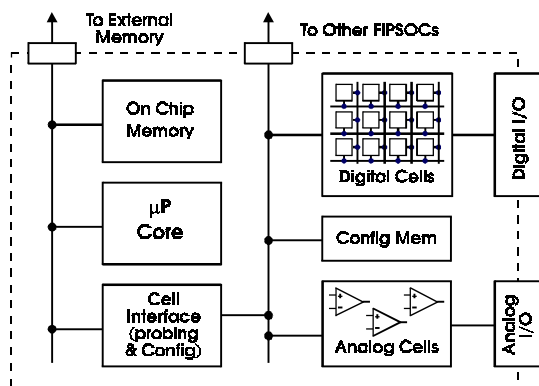


Fig.1: Block diagram of the FIPSOC chip

The chip, as depicted in Fig. 1, is a mixed signal field programmable device with an on-chip microcontroller. It includes a Field Programmable Gate Array (FPGA) of large granularity, synthesis targeted, Look-Up Table based programmable blocks, a set of fixed-functionality yet configurable analog cells (such as amplifiers, filters, comparators, ADC/DAC, etc), and a standard (8051) microprocessor core with RAM memory and some peripherals. The microprocessor is responsible for configuration (the configuration memory is mapped on the address space) and general purpose user programs. Furthermore, two configuration contexts are stored (the configuration memory is duplicated) and the user can instantaneously swap them, so the chip (or a selected set of cells) can be reconfigured with just a microprocessor write command.

The programmable digital and analog blocks are well defined and are separated from one another due to noise immunity considerations. Nevertheless, the different interfaces between these blocks themselves and to the microprocessor provide a very powerful interaction between software, digital hardware and analog hardware: The microprocessor can probe in real time actual analog (dynamically reconfiguring the ADC block) and digital (as memory locations) signals within the FPGA, then communicate to a (PC) workstation thru the serial port. The user gets then a real time digital oscilloscope, a logic analyzer and a test board onto which he can map mixed signal designs, just with the FIPSOC chip and a PC. The advantage of this approach relies upon the fully integrated design and prototyping methodology that the user can follow with such a system, because he can download his application onto the programmable hardware and then use the internal microcontroller to probe it in real time (both digital and analog). A powerful integrated set of user-friendly CAD tools is provided, with the final target of letting the user specify, simulate, emulate (probe in real time) and map the complete design on to a single chip using one design environment. Also, a suitable library has been developed providing a very easy path for migration to ASIC after the prototyping phase.

The chip has been designed using a full custom methodology for the FPGA and the analog area, and a synthesized *soft core* for the microcontroller. A 0.5μm triple metal layer CMOS 3V process provided by ATMEL ES2 was chosen to implement the first generation of this device.