

Panel Session

What Will Be the Right Test Methodology for the Year 2005?

Moderator

Keith Baker, Philips, The Netherlands

Participants

Birger Schneider, Microlex, Denmark

Piet De Pauw, Alcatel-Mietec, Belgium

Tom Williams, IBM, USA

Bob Grubel, TI, USA

Steven Athan, Univ. Florida, USA

Each year the complexity of VLSI systems increases and test development consumes a major portion of the development cycle. The goal of this panel is to discuss the roads that will get test methods into the future. Questions that have to be answered are : what will be the key problems when evolving towards deep-submicron testing , what will be the impact of high level design and synthesis techniques on test issues, how will we cope with systems on silicon combining hardware/software and digital/analog, how will a system test strategy cope with the combination of heterogeneous test approaches (such as Iddq, Bist, Scan) for the different components on a single chip, how can the quality of the test process be improved for devices of more than hundred million transistors. The result of this panel should help the universities and research institutes to identify what will be the requirements of leading (and bleeding) edge industrial applications for the year 2000.