A New Quality Estimation Methodology for Mixed-Signal and Analogue ICs

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Abstract

IC product quality is commonly described as the faulty device level at shipment and is becoming an increasingly important metric in the Microelectronics Industry. This paper presents and demonstrates a quality estimation approach based on Inductive Fault Analysis for mixed-signal and analogue ICs, that quantitatively models the quality related parameters prior to production. It is shown how the approach can be used to optimise the manufacturing test program.

1. Introduction

IC product quality, commonly described as the faulty device level at shipment in parts per million (ppm), is a function of a number of interrelated processes including the manufacturing environment and technology parameters, the design, design-for-test (DfT) features, the test approach, and the test evaluation method, see figure 1. The ability to model each of these processes for quality optimisation is therefore critical. For example, dust particles or faults in the masks for the photo-lithographic process may cause faults within the IC. It is therefore necessary to model these effects together with the technology parameters that define the faults. The design has an impact on the IC product quality since there are a number of circuit and system design structures which are inherently difficult to test [1]. Where circuit parts that are difficult to test exist, Design-for Test (DfT) techniques can be incorporated [2][20]. The optimum test approach is critical to IC product quality as a poorly defined approach is likely to achieve poor fault coverage and hence contribute to the faulty device level (FDL). It is therefore necessary to be able to access the effectiveness of a particular test strategy through pre-production fault simulation [15].

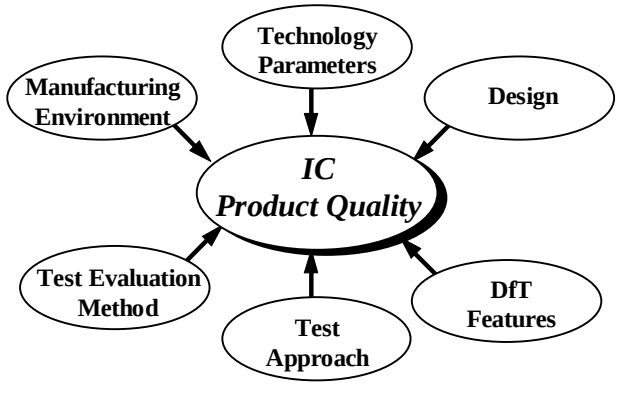

Figure 1: Different Influences on IC Product Quality

Achieving high IC product quality whilst maintaining cost effectiveness requires the optimisation of all the above factors and their interdependence. Traditional approaches involve life testing or field return analysis. These approaches are post manufacture techniques and are carried out after

- The manufacturing environment has been set-up
- The mask sets for the IC have been produced
- DfT strategies and the test program have been defined

It is usually expensive and often impractical to undertake modifications to obtain a higher test effectiveness and lower test cost after the manufacturing environment has been set-up. A modelling and simulation approach is therefore required to accurately and rapidly identify limitations in the manufacturing test prior to production. This paper presents a product quality estimation approach for mixed-signal and analogue ICs based on Inductive Fault Analysis (IFA) which takes quality related issues into account for manufacturing test analysis and optimisation prior to production. Pro-active test evaluation and test optimisation is presented which has many advantages over the conventional re-active procedures implemented to date. The procedure has been integrated

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into the Cadence DFWII design environment to support the integration of a "Design for Manufacture" strategy into the design cycle. This strategy provides the designer with support for optimising the design for test as well as performance and defining an optimal test strategy.

The paper is organised as follows. Section 2 reports on related work, both on approaches to statistical defect level prediction as well as on applications of IFA based fault simulation. Section 3 presents the modelling and simulation of the manufacturing test approaches for mixed-signal circuits and systems. An example of how the product quality estimation approach can be used to optimise the test strategy for a 2nd-order Sallen-Key filter is presented in sections 4 and 5. The IFA statistics and simulation results are given in section 6. Section 7 discusses limitations as well as advantages of the experiments undertaken. Section 8 summarises the work and presents conclusions.

2. Related Work

2.1 Defect Level as a function of Yield and Fault Coverage

Williams and Brown [3] published on "defect level as a function of fault coverage". Their underlying concept is that only a subset, *m*, of the complete set, *n*, of all possible stuck-at faults in a digital circuit are considered in fault simulations. They established a relationship between the defect level, the *m/n* ratio and the yield of the process. "The Williams-Brown model makes several assumptions, which can roughly be divided into four distinct groups" [4]:

1. *"All faults have the same probability of occurrence"*. This cannot be considered accurate. IFA based fault list generation, for example, which takes circuit layout as well as process and manufacturing parameters into account, assigns weighting factors to estimate the probability of occurrence.
2. *"The presence of a fault is independent of the presence of other faults"*. In reality fault occurrences are not independent of how many (and which) other faults are also present on a chip. Huisman [4] discusses this fault clustering phenomena in detail.
3. *"Fault Detection are independent events"*. This assumption is common to all quality estimations.
4. *"The list of possible faults is complete and accurately modelled"*. There are numerous reports that the stuck-at fault model does not describe all possible faults in digital circuits. Huisman [4] assumes that "there are roughly as many modelled faults as there are unmodelled ones", if the stuck-at fault model is applied to digital circuits. For mixed-signal circuits fault simulation results are a strong function of the fault model utilised [5].

It can be seen that many of the assumptions on which the defect level prediction is based are not valid. More refined models have been presented which only partially help to overcome some of the limitations [6][7][8][9]. Williams and Brown [3] predicted defect levels by extrapolating fault simulation results which only consider a subset of all possible faults and by taking manufacturing yield information into consideration. In comparison, the IC product quality estimation approach utilised in this paper is different in that it utilises more realistic assumptions and therefore helps overcome some of the limitations of previous approaches in that it simulates a (quasi) complete fault list where the faults are statistically weighted.

Caunegre and Abraham [10] reported on "achieving simulation-based test program verification". They used fault simulation to analyse how well their test environment can test a chip. This allows for DfT optimisation before the chip is introduced to production. The work presented in this paper is an extension in that it utilises layout extracted fault lists which allow quantitative prediction of the probability of faulty devices escaping all manufacturing tests. The approach in this work leads to a realistic IC product quality metric.

2.2 Application of IFA based Fault Simulation

Realistic fault modelling methods [11], which consider manufacturing defects in the circuit layout, were initially developed to model the yield of an IC as a function of the manufacturing process, the IC technology involved and the device itself. This approach is also referred to as Inductive Fault Analysis (IFA) [12][13]. For this project, VLASIC [14] has been used as the IFA tool. Over the last few years IFA has been utilised for a number of other applications and purposes, see figure 2.

For instance, IFA generated fault lists have been used for analogue fault simulation [15]. Here, limitations of inaccurate fault models have been overcome by using realistic, layout dependent defect modelling techniques. They have a "weighting" factor assigned to each fault describing the probability of occurrence. Furthermore, IFA has been utilised for qualifying and optimising DfT schemes [5] and to perform testability analysis [16][17].

Applications of IFA include the optimisation of IC layout of mixed-signal circuits [18]. Undetectable and, therefore, critical faults can be localised in the layout. This allows

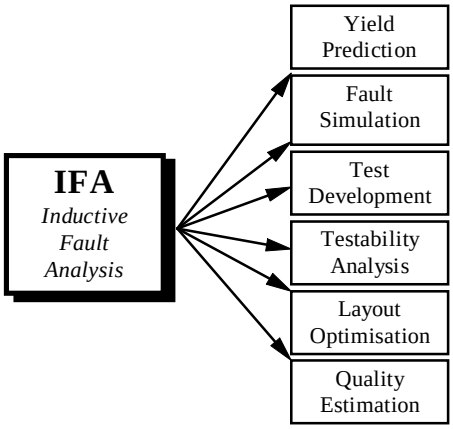

Figure 2: Different Applications for IFA

optimisation of the layout to reduce the probability of the occurrence of faults which cannot be detected with the test approach in use. In this paper, another application of IFA is presented. IFA generated weighted fault lists together with fault simulation and simulation analysis are used to establish the Faulty Device Level (FDL), see equation 3, which is an increasingly important quality metric for IC products.

3. Modelling and Simulation of the Manufacturing Test Approaches for Mixed-Signal Circuits and Systems

The IC product quality estimation approach is depicted in figure 3. All parameters which influence the IC quality, commonly described as the probability of faulty devices shipped, are considered.

The *Inductive Fault Analysis (IFA)* approach is utilised to model spot defects which are introduced into the silicon die which result from imperfections in the manufacturing environment and the process technology. The IFA process statistically models the number of defects which may occur in a product run (eg. 1,000 / 1,000,000 pieces). All defects are analysed that cause a fault in the CUT, and hence a netlist variation, and are weighted according to their probability of occurrence. The output from the process includes information on the *yield* of the manufacturing process and a *weighted fault list* which is used as entry to the fault simulations. During *fault simulation*, the corresponding simulation models are injected into the netlist. The *test approaches* considered for the manufacturing tests are applied to the CUT and the simulation responses captured for *simulation analysis*. The *test evaluation methods* define how the test response data is evaluated and which thresholds to apply for go/no-go decisions. The *testability analysis* reveals untestable circuit parts and provides information on the test, such as testing time, test requirements, and the cost of test implementation.

Quality information on the complete manufacturing and test process is obtained. The fault coverage figure, which is defined as the number of detected faults divided by the total number of faults simulated, is obtained from the IC product quality estimation approach with improved accuracy by considering the probability of a fault occurring in a manufacturing process (equation 1).

$$FC = \frac{\sum_{n=1}^{N} F_n \cdot W_n}{\sum_{n=1}^{N} W_n} \cdot 100\% \quad \ldots\ldots\ldots (1)$$

Here, *FC* is the weighted fault coverage, W_n represents the total number of circuits in the batch affected by fault *n* and N is the total number of faults across all circuits. F_n=1, if a fault *n* is detected by the target test program. An undetected fault *n* is described with F_n=0.

A test program may be composed of different tests. $F_{n,m}$ is the test result of test *m* for fault *n*. The fault detectability of

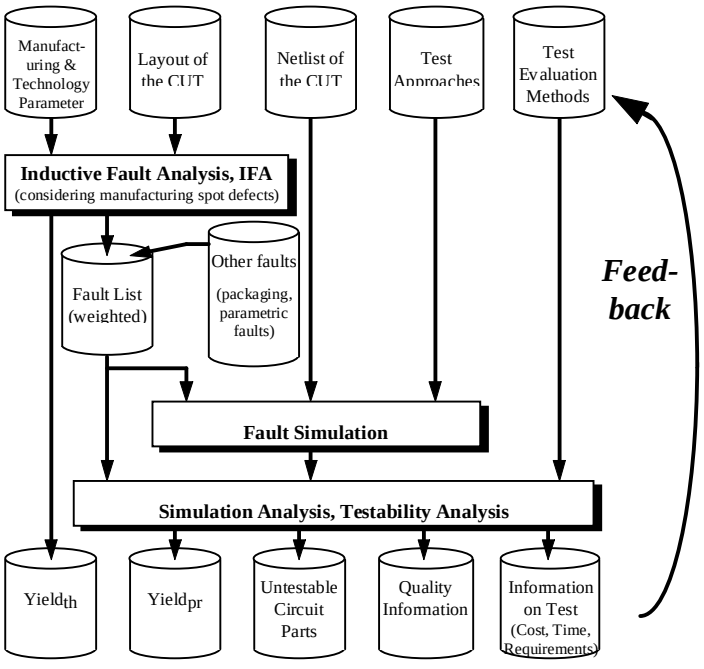

Figure 3: The IC Product Quality Estimation

a fault *n* tested by a test set is described:

$$F_n = \max_m F_{n,m} \quad \text{……. (2)}$$

As the IC product quality estimation approach depicted in figure 3 models realistic defects in a manufacturing process, it is possible to simulate yield figures. A "theoretical" definition of yield [3], Y_{th}, is the ratio of non-faulty devices to the total number of manufactured devices, *B*. This value can be directly obtained from the IFA tool. A more "pragmatic" definition of yield, Y_{pr}, is the ratio of the number of devices tested good to the total number of manufactured devices. This value is obtained from testability analysis (figure 3) and equals the sum of the number of good devices and faulty devices that have escaped all tests. Furthermore, the IC product quality estimation approach allows the modelling of the probability of a faulty device escaping all manufacturing tests. This *Faulty Device Level, FDL*, is defined as:

$$\text{FDL} = \frac{\text{number of faulty devices at shipment stage}}{\text{total number of devices shipped out}} \cdot 1e6 \text{ ppm}$$

……. (3)

and can be calculated with:

$$\text{FDL} = \frac{\sum_{n=1}^{N} W_n - \sum_{n=1}^{N} F_n \cdot W_n}{B - \sum_{n=1}^{N} F_n \cdot W_n} \cdot 1e^6 \text{ppm}$$

$$= \frac{100 - \text{FC}(\%)}{100} \cdot \frac{\sum_{n=1}^{N} W_n}{B - \sum_{n=1}^{N} F_n \cdot W_n} \cdot 1e^6 \text{ppm}$$

……. (4)

In this way *FDL* can be estimated taking manufacturing, design and test into consideration. Equation 4 identifies that not all faulty devices ($\sum W_n$) contribute to the FDL figure but only those that escape all tests ($\sum W_n - \sum F_n.W_n$) and are shipped to the customer. Similarly, the total number of devices shipped out ($B - \sum F_n.W_n$) will be less than the total number of manufactured devices, *B*, since the tests remove faulty devices detected ($\sum F_n.W_n$) by the test program.

Assumptions on which the IC product quality estimation approach is based:

1. *"The list of possible faults is complete"*. The IFA analysis generates a weighted fault list which is substantially smaller than, for example, complete stuck-at fault lists, and can, therefore, be completely simulated.
2. *"The faults are accurately modelled"*. IFA analysis allows much more accurate and realistic fault modelling than traditional schematic based fault models.
3. *"Faults are weighted according to their probability of occurrence"*. The IFA analysis utilises manufacturing statistics as well as technology parameters in addition to layout information to accurately model and predict the probability of occurrence.
4. *"Multiple fault occurrence is possible"*. The IFA approach allows manufacturing defects to be modelled such as multiple short-circuits.

The IC product quality estimation approach models statistically relevant manufacturing defects, i.e. spot defects, and simulates manufacturing test to obtain information on the rate of faults which escape the manufacturing tests. This approach can be applied to IC subsystems, i.e. macros or function blocks. Complete and complex IC systems may be analysed using a "divide-and-conquer" approach. It is important that the macro test then reflects system level aspects, i.e. considers the limited accessibility of embedded macros within a large system.

4. Test Specification Development for Optimal Product Quality

The IC product quality estimation approach can be used for test program optimisation. The strategy adopted here is to extend the macro test [19] concept to mixed-signal and analogue circuits. It is assumed that the design can be partitioned at the functional and layout levels into distinct macros and interconnect, and each functional block can be tested separately by either externally applied stimulus or Built-In Self-Test (BIST). This is a realistic option for the next generation devices due to recent developments in DfT strategies including 1149.4 [20], proprietary internal analogue test buses and other custom structures which allow improved access and observability of embedded functions [2]. The concept is to define a "virtual test harness" for each cell, as shown in Fig 4. It is likely that, for implementation into a Computer Aided Test (CAT) environment, additional information will be required including a simulation model and fault list.

This format will provide all that is required to perform a testability analysis at the system level and define the chip level test program to ensure all necessary inputs can be applied and test responses sampled. For this strategy to be

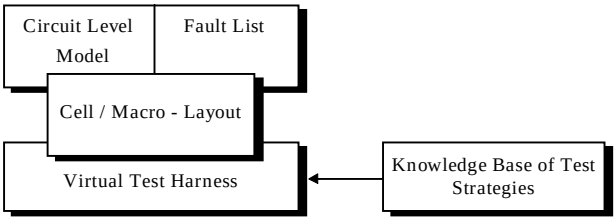

Figure 4 : Virtual Test Harness Concept for Mixed-Signal and Analogue Macro Test

effective, a knowledge base of possible test strategies is required.

To demonstrate this procedure, an example design has been chosen. This design, a 2nd-order, continuous time unity gain Sallen-Key low-pass filter module with a cut-off frequency of 39.4kHz, is a key component of a mixed-signal design library, (see figure 5). As the filter is a macro embedded into a larger system, there is only limited access to it. The single ended input and output are assumed to be freely accessible. The power down mode, controlled via the *PD* nodes, is utilisable. Furthermore, it is assumed that all other macros in the IC can be set into a power down mode so that the power supply current of the CUT can be measured on its own. No internal nodes are accessible for test purposes. The op-amp is a "state-of-the-art", 50 transistor, rail-to-rail two-stage amplifier for low-voltage applications.

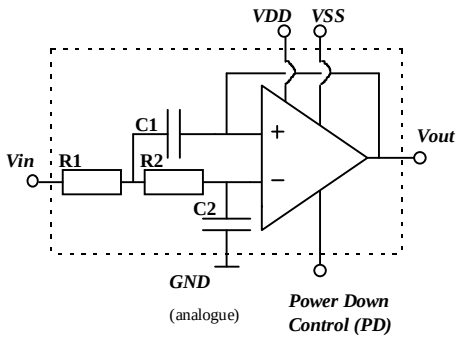

Figure 5: 2nd-order Low-Pass Filter to demonstrate the IC Product Quality Estimation approach.

5. Functional as well as Parametric Test Approaches to maximise Test Effectiveness

A number of test approaches were assessed in order to maximise test effectiveness. The aim was to find the combination of tests which optimised test exhaustiveness, minimised the number of faults which escaped all tests whilst minimising the test time. Beside the "traditional" functional tests, such as measuring Total Harmonic Distortion (THD), output offset, gain and phase margins, more "unconventional", parametric tests were utilised, such as power supply measurements with the op-amp simulated in power-down mode. Table 1 gives an overview on the different types of tests considered. The parametric tests allow detection of faults which escaped the functional tests. However, acceptable coverage is not possible without selected functional tests.

	Test Ident	Test Measure	Op-Amp Mode
Parametric Test	A	DC Offset	Power-Down Mode
	B	DC Offset	Operational Mode
	C	I_{DDQ}	Power-Down Mode
	D	I_{DDQ}	Operational Mode
	E	I_{SSQ}	Power-Down Mode
	F	I_{SSQ}	Operational Mode
Functional Test	G	THD	Operational Mode
	H	Voltage Gain at 100Hz	Operational Mode
	J	-3dB Frequency	Operational Mode
	K	Voltage Gain at 50kHz	Operational Mode
	L	Voltage Gain at 500Hz	Operational Mode
	M	Roll-Off, (dB/decade), 50kHz and 500kHz	Operational Mode

Table 1: Functional and Parametric Test Approaches for maximum Testability and optimum IC Product Quality

6. Simulation Results

Table 2 gives an overview of the statistics from the defect extraction process on the 2nd-order filter module. A batch of 100,000 devices were assumed from which a weighted fault list was created as input to the fault simulation and testability analysis, see figure 3. The IFA extracted faults were modelled as either electrical shorts or opens. The majority of identified faults were shorts and modelled in the fault simulation using resistance values obtained from bridging fault measurements in a CMOS process [21]. This utilised two short resistance values (minimum and maximum) to model variations due to defect form and location. Several models have been suggested to model the open faults [22][23][24]. For this analysis, a simple model was used, consisting of a high value resistance with a single value of 10MΩ.

Figure 6 shows fault simulation results on the test effectiveness of the different tests described in table 1. All

fault simulations were performed at transistor level using HSPICE. None of the tests were capable of achieving "reasonable" fault coverage figures alone. Only a combination of the different tests allowed for fault coverage figures above 98% which translates to Faulty

IFA Statistics	
100,000	circuits assumed in manufacturing batch
113,418	defects scattered onto the circuits
24	different types of spot defects considered
1,469	faults identified (= defects which resulted in a netlist variation)
1,461	faulty circuits considered
65	"weighted faults" simulated that described all 1,469 faults

Table 2: Inductive Fault Analysis performed on the 2nd-order Low-Pass Filter. The IFA tool is VLASIC [14].

Device Levels of better than 300ppm. Fault detection thresholds were set by considering both the fabrication process variations and ATE (automatic test equipment) resolution. Monte-Carlo simulations were run to model process variations. Figure 7 shows the FDLs for a sub-set of all possible test combinations. The conversion from fault coverage figures to faulty device levels is given in equation 4. Here, combinations of tests were available which allowed detection of all possible faults (derived through IFA analysis). The virtual test harness for this circuit could therefore consist of a measurement of voltage gain at 100Hz supplemented by an I_{DDQ} / I_{SSQ} test in both power-down and operational modes, or a more thorough functional test (THD, voltage gain and -3dB frequency) supplemented by an I_{DDQ} test in power-down mode only. The choice will depend on economic factors including test time and resource requirements. In this case, without BIST, the I_{DDQ} / I_{SSQ} tests are likely to take longer,

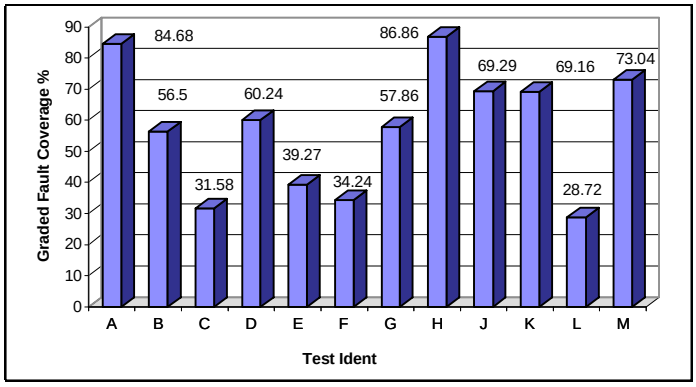

Figure 6: Fault Coverage Figure for the different Manufacturing Tests for the 2nd-order Low-Pass Filter Module, based on a weighted IFA fault list.

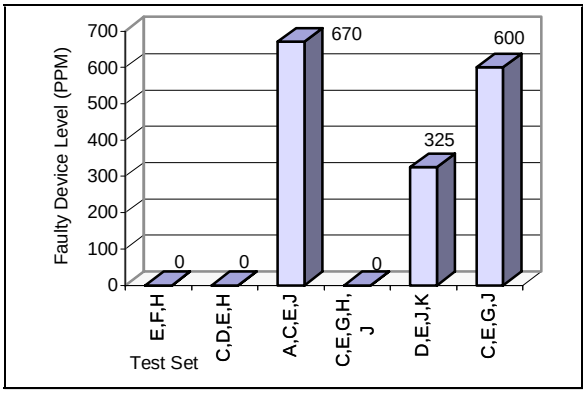

Figure 7: Faulty Device Levels (FDL) for different combinations of Tests (see table 1).

however the THD and -3dB frequency measurements will require expensive mixed-signal tester resources.

7. Discussion

The IC product quality estimation approach has been applied to a 2nd-order low-pass filter within a mixed-signal design library. The combination of different test approaches led to acceptable defect levels. However, it needs to be noted, that even "single figure ppm levels" for the low-pass filter do not necessarily satisfy current demands on quality as the IC consists of many such macros that may all contain undetectable faults which have a cumulative effect on the defect level. Furthermore, there are other sources of quality degrading manufacturing faults which have not been considered for the demonstrator such as:

- *Packaging effects*. Manufacturing faults caused, for example, from erroneous bonding, and wrong handling need also to be screened out by the manufacturing tests. They can be modelled externally and included in the fault simulations, see figure 3.
- *Parametric process deviations.* The IFA process considers only manufacturing spot defects and no parametric deviations which may result for example in transistor mismatch. However, such effects can also be modelled and included in the fault simulations.

Beside the sources of manufacturing faults which have not (yet) been considered in the IC product quality estimation approach presented in this paper there are some limitations in the experiments which are listed below:

- *Complexity of approach*. Simulation times become excessive, especially for discrete-time mixed-signal circuits such as switched-capacitor, switched-current, or sigma-delta modulator circuits. The "divide-and-conquer" approach helps to tackle the complexity
- *VLASIC is not really a mixed-signal tool*. VLASIC which is the underlying software tool for the IFA analysis on the demonstrator circuit does not model manufacturing defects accurately for some devices, especially for resistor snakes, etc. Spot defects may result here in a deviation of its nominal value. VLASIC, however, identifies only defects as faults which result in a netlist alteration. Therefore, techniques have been implemented which overcome the problem and which allow simulation of parametric deviations caused by spot defects on mixed-signal circuit elements such as resistor snakes.

Despite the (possible) limitations and shortcomings of the IC product quality estimation approach presented in this paper, there are many advantages which make this technique valuable, important and useful to be integrated into the IC design flow:

- *Reduced time to market*. Modelling and simulating the manufacturing process and production test allows identification of quality degrading effects before the IC product is introduced into production. Test optimisation can, therefore, be pro-active rather than re-active.
- *Quantitative results obtained*. Fault coverage figures as the traditional figure to quantify fault simulation is not an acceptable measure for test engineers and production managers. For example, there is an ongoing discussion on "How much above 100% fault coverage?" it should be targeted if the underlying modelling concept is based on the stuck-at fault model [4]. The approach presented in this paper derives test effectiveness metrics that are equivalent to those used in manufacturing.
- *Cost benefit*. Modelling and simulating the impact of a) manufacturing defects on the CUT behaviour, b) the testability of a CUT, and c) the test effectiveness of the manufacturing test allows identification of the quality degrading influences in the product life cycle from design via manufacture and test to shipment, this before high costs occur such as delayed time to market, redesign of CUT, liability for field returns, or additional and expensive tests.
- *"De-mystifies" non-conventional mixed-signal test generation*. Novel, non-functional (parametric) test approaches have been successfully utilised to increase test exhaustiveness. However, it needs to be justified for each case when and to what extend parametric tests, such as I_{SSQ} measurements for mixed-signal devices, can replace (lengthy and, therefore, expensive) functional tests. The IC product quality estimation approach presented in this paper is ideally suited to qualify such test approaches for introduction into the manufacturing environment.
- *Automatable approach*. The IC product quality estimation approach is highly automatable and integratable into the design flow and into standard IC CAD environments. The cost for performing such an IC product quality estimation, in terms of man month required can, therefore, be drastically reduced.
- *Adaptable to new technologies*. Because the IC product quality estimation approach utilises defect statistics directly from the manufacturing environment, it can easily be adapted for new manufacturing processes and new technologies. Forthcoming designs in deep sub-micron technologies as well as microsystems can be evaluated using this quality estimation approach.

8. Conclusions

A modelling and simulation approach which leads to an estimation of the IC product quality, described by the rate of faulty devices which escape all manufacturing tests, has been presented in this paper. It utilises Inductive Fault Analysis (IFA) to extract weighted fault lists which are dependent on the manufacturing and technology parameters as well as on the device layout. Fault simulation and testability analysis take the IFA generated fault list together with the device netlist to model the complete manufacturing test process. The various test approaches are simulated and the simulated measurement data evaluated to obtain the quality information which indicates how many faulty devices are shipped out.

This IFA based fault simulation approach helps to optimise IC product quality prior to production. Other advantages are reduced time to market, lower defect levels at shipment stage, reduced cost for test, optimised DfT features and confidence in product quality.

9. Acknowledgements

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