

Testing scheme for IC's clocks

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Abstract

This paper proposes a testing scheme to detect abnormal skews between clock signals inside digital synchronous ICs. The scheme is based on a new CMOS sensing circuit whose compactness and testability with respect to a large set of failures make it suitable for both off-line and on-line testing.

1 Introduction

The scaling of interconnections and the increasing of both speed and size of digital circuits have made critical the distribution of synchronization signals throughout the chip. Unbalanced paths may result in large clock skews possibly pushing the circuit out of timing specifications. As a consequence, the yield and reliability of circuits may be degraded.

Several techniques have been developed to deal with this problem: the target of zero clock skew is typically achieved by the insertion of buffers to control delays and/or by proper routing algorithms [1, 2, 3, 4, 5]. In particular, buffer insertion implies extra delays, so that an optimal tradeoff between the extra delay and skew minimization should be found, while zero-skew clock signals' routing presents practical problems when the circuit size increases. As a matter of fact, these techniques are typically used together: the clock distribution tree is implemented in a hierarchical way, with buffers driving optimized interconnection networks.

Although these efforts have provided reliable clock tree design methodologies, several kinds of failures may still affect the clock signals. In particular, circuit parameter fluctuations, inaccuracies in the delay models used to drive the clock routing process, cross-talk faults and environmental failures (typically due to wire coupling with off-chip sources of noise) may degrade the reliability of clock operations. Conventional approaches may be ineffective to test with respect to these kinds of faults; in fact, a small fraction

of them can be classified as permanent, while the others have to be considered (intrinsically or practically) as transient. In addition, conventional testing procedures are often oriented to faults in IC's logic, while the detection of faults affecting clock signals is commonly treated as a side effect. In fact, it is easy to verify that a clock distribution fault resulting in one or more flip-flops' delayed sampling cannot be immediately assimilated to delay faults inside the combinational part of the circuit, because a delayed flip-flop's response may be masked by its delayed sampling. At our knowledge, no work explicitly addresses the problem of detecting faults affecting the clock signals.

On the basis of these considerations, we propose an original approach to the detection of faults affecting the clock distribution network. The presented scheme can be used in off-line, conventional testing applications, as well as in on-line, high-reliability targeted (self-checking [6, 7] and fault tolerant [8]) ones.

The scheme is based on a novel sensing circuit, that can be used to reveal the presence of abnormal skews between the edges of two input signals. The basic idea is to individuate couples of critical wires in the clock distribution trees (i.e. signals expected to present a high probability of large skews), and to connect each of such couples to a sensing circuit with balanced lines, which provides an error indication when the skew between the monitored clock signals exceeds its sensitivity.

The proposed sensing circuit is very simple and its sensitivity can be easily settled to account for different tolerances on the clock skew. In addition, the circuit can be used in self-checking circuits, because of its high self-testing capability.

This paper is organized in the following way: section 2 describes the proposed sensing circuit, its operations and its application to a typical clock distribution scheme. The testability of the proposed circuit is analyzed in section 3, and conclusions are drawn in

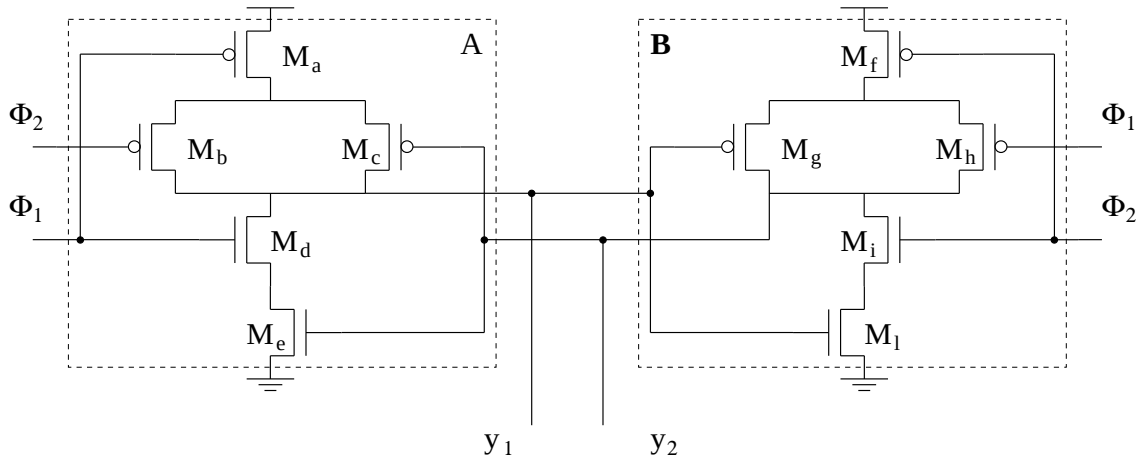


Figure 1: Sensing circuit proposed in this work for testing clock distribution. Two signals Φ_1 and Φ_2 branching from the same clock generator are checked to detect the presence of abnormal skews.

section 4.

2 Sensing circuit scheme

The proposed sensing circuit (Fig. 1) consists of two symmetric blocks (A and B) closed in a feedback loop. The inputs of such blocks are the two monitored clock signals (Φ_1 and Φ_2), that are supposed to come, through different paths, from the same clock generator. The outputs of A and B (y_1 and y_2) provide an error indication (01 or 10) in the presence of abnormal skews between the rising¹ edges of the monitored signals, while in case of correct clock signals, A and B simply act as inverters.

In the remainder of this section, we will illustrate the behavior of the proposed circuit in both such cases.

Let us suppose that no skew exists between the rising edges of Φ_1 and Φ_2 : in this ideal case, when both clock signals are low, the pull-up networks of both blocks are ON and their outputs are high. When the two clock signals switch (simultaneously), both pull-ups are turned OFF, while the pull-down networks are turned ON, thus discharging the block output capacitances (Fig. 2). It should be noticed, that, in this case, the voltage of y_1 and y_2 cannot fall below the n -channel conductance threshold, because of the feedback between the two blocks. If this cannot be accepted, a suitable feedback inverter driving a weak pull-down n -channel transistor can be added to each block to provide full-swing performance.

In the presence of skews, instead, if the rising transition of Φ_2 is delayed with respect to that of Φ_1 , y_2

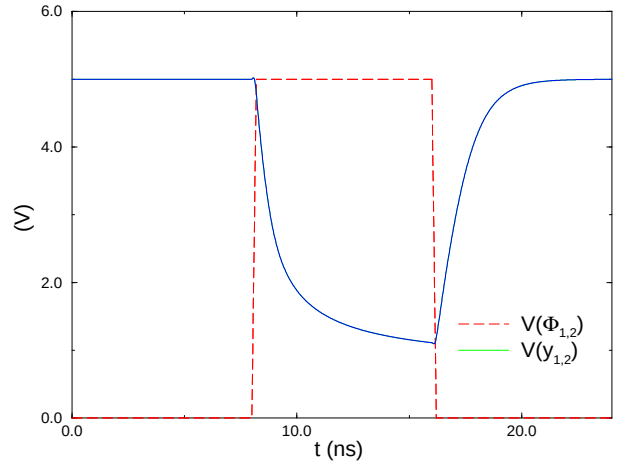


Figure 2: Input and output waveforms of the proposed sensing circuit in the ideal case of no skew between the signals.

will not switch to a low logic value, thus providing an error indication ($y_1, y_2 = 01$). Of course, a transition of Φ_1 delayed with respect to that of Φ_2 is revealed by the output configuration (10).

In particular, when Φ_1 rises with Φ_2 low, block A starts to switch to a low output value, while the output of B is in a high impedance state still keeping its high value. If the signal y_1 has reached a low value when also Φ_2 rises, the pull-down of B cannot be turned ON because the transistor driven by y_1 (M_l) is OFF. Hence, y_2 maintains a high logic value, thus providing an error indication ($y_1, y_2 = 01$), that holds for a time long enough (half of the clock period) to allow the detection of the problem by means of a suitable (synchronous or asynchronous) network (Fig. 3).

¹ This circuit can be used if flip-flops sample on the rising edge, otherwise a dual circuit should be used.

This condition is always verified when the skew (τ) between the clock phases is larger than the delay (d) required by the output signal y_1 to reach a low value. When this is not the case, y_2 has an incomplete falling transition and reaches a minimum voltage value (V_{min}). In this case, however, the detection of the skew is still possible by using a proper threshold when evaluating the sensing circuit response. By acting on such a threshold voltage (V_{th}) and/or on the delay of the sensing circuit blocks, it is possible to set a suitable tolerance interval. In particular, the sensitivity of the proposed circuit increases with the decrease of V_{th} and the delay.

In order to explore this tradeoff and the sensing circuit accuracy, electrical level simulations have been performed considering a $1.2\mu m$ implementation of the sensing circuit. To this purpose, an additional capacitance (C_L) has been connected to y_1 and y_2 to represent different loading conditions.

In particular, the values of V_{min} have been evaluated as a function of the skew between the clock signals, by considering different values of load capacitance and different slopes of the clock signals. In order to evaluate the threshold used to discriminate high (erroneous) voltage values, we have supposed that a gate with logic threshold equal to $V_{DD}/2$ is used to interpret the sensing circuit response. A worst case variation of 10% has been considered to account for circuit parameter fluctuations, thus resulting in $V_{th} = 2.75V$.

The achieved results are shown in Fig. 4. For values of τ such that $V_{min} > V_{th}$, y_2 is interpreted as a high logic value, thus providing an error indication: such values of τ (to be referred as τ_{min}) depending on the values of the load capacitance and vary from 0.09ns to 0.16ns. In this regard, it is interesting to notice that the circuit is rather unsensitive to the slope of clock signal waveforms: in fact, for each load value, we have considered values of the clock slew (i.e. the rise time of Φ_1 and Φ_2) ranging from 0.1ns to 0.4ns and, as can be seen from the figure, the resulting curves are almost indistinguishable.

In addition, to account for the effect of random fluctuation in IC parameters, we have performed a set of Montecarlo simulations by supposing a uniform distribution (with 0.15 as relative variation from the nominal value) of the circuit parameter and of C_L . Moreover, the slew of the monitored clock signals has been supposed to have an uniform distribution in the interval $[0.1ns, 0.4ns]$. Both the input slews and the load have been considered independent, in order to account for asymmetric conditions.

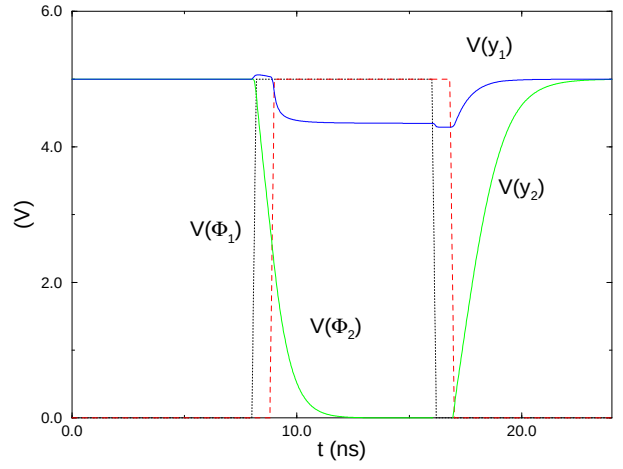


Figure 3: Input and output waveforms in the presence of a skew between the monitored clock signals.

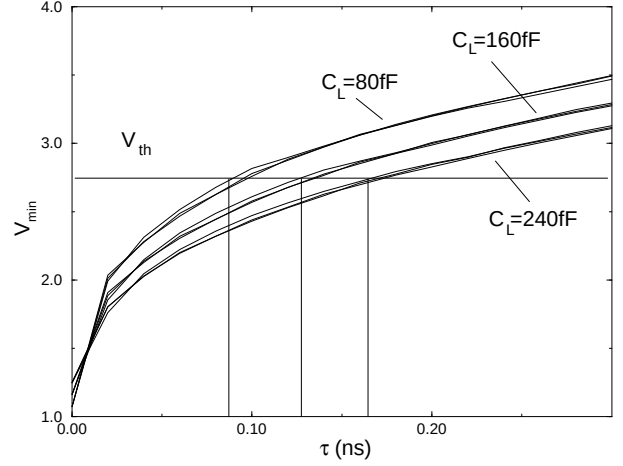


Figure 4: Minimum voltage reached by the sensing circuit output as a function of the skew between the two monitored clock phases evaluated for different values of load capacitance. For each value of load capacitance, different values of clock slope have been considered. Vertical lines individuate the values of sensitivity of the sensing circuit.

The achieved results are illustrated in Fig. 5 showing the scatterplot of V_{min} as a function of τ . As can be seen, the proposed circuit is slightly sensitive to parameters variations. From a quantitative point of view, for each considered nominal value of C_L , we have evaluated the probability (p_{loose}) of loosing an error indication (i.e. $\tau > \tau_{min}$ and $V_{min} < V_{th}$) and that (p_{false}) of having a false error indication (i.e. $\tau < \tau_{min}$ and $V_{min} > V_{th}$) (Tab. 1).

As regards the use of the sensing circuit inside complex CMOS ICs, two criterions have to be used in order to individuate the couples of signals to be checked:

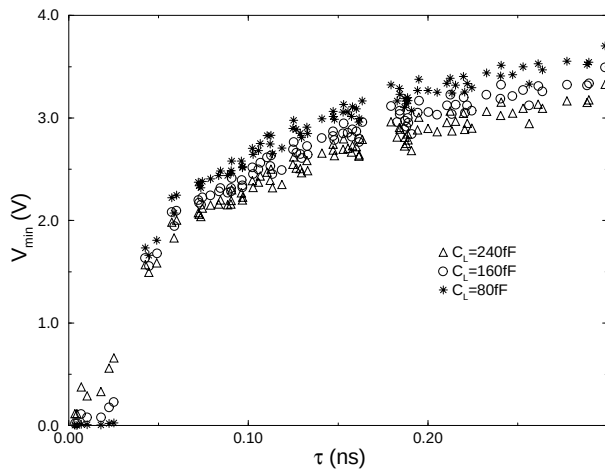


Figure 5: Scatterplot of the V_{min} values as a function of τ in the presence of random circuit parameter variations.

C_L	p_{lose}	p_{false}
80fF	0.12	0.0
160fF	0.04	0.01
240fF	0.02	0.02

Table 1: Probability of losing (p_{lose}) an error and of generating a false error indication (p_{false}).

1. the skew between them must be critical (accurate timing analysis tools should provide these data);
2. they must be close enough to each other to allow for a suitable (i.e. balanced) connection to the sensing circuit.

These tasks are not analyzed in this paper, but, as can be seen in the example of Fig. 6, the symmetries in the clock distribution scheme can be suitably exploited to satisfy condition 2.

Once the sensing circuits have been placed, a suitable circuitry should be used to bring up the answers of such circuits. To this purpose, simple error indicators [9] capable of latching on error indications can be used, and their response could be driven through a scan-path (in the case of off-line testing) or could feed a checker (in the case of on-line applications).

3 Testability of the sensing circuit

In both off-line and on-line (self-checking) applications, the testability of the proposed sensing circuit is fundamental to ensure the reliability of operations of the whole testing scheme. In the case of on-line applications, it is important to ensure that the proposed scheme features on-line self-testing ability with respect to its internal faults in the presence of fault-free input

stimuli. In the considered kind of applications, this condition has to be verified also in the case of off-line testing, because the clock signals cannot be controlled independently from each other.

In this work, the testability of the proposed sensing circuit is analyzed by means of electrical level simulation, with respect to a set of realistic faults, including stuck-ats, transistor faults and bridgings [10].

In the case of node stuck-at faults, it has been verified that the proposed circuit provides an error indication for each possible fault, so that the sensing circuit is 100% testable.

As regards transistor stuck-open faults, it has been verified that all faults of this kind are detected apart from those affecting the transistors M_c and M_g that, however, do not mask the presence of abnormal skews at the inputs of the sensing circuit. The circuit is still able to detect such skews even if the error indication is not statically latched. Such faults can be avoided by implementing the transistors by means of suitable layout schemes [11].

In the presence of transistor stuck-on faults, instead, it is known that CMOS circuits exhibit a typically analog behavior [12]: conflicting networks produce intermediate faulty voltages, additional delays and abnormal static current assumption. In the context of this work, a stuck-on fault is considered detected if it produces a faulty voltage that is interpreted as a logic error by the logic driven by the sensing circuit (i.e. the faulty voltage lies from the opposite side of V_{th} with respect to the fault-free value).

Under these conditions, it has been verified that only the 60% of all the stuck-on faults are detected. In particular, the stuck-ons affecting the parallel pull-up transistors ($M_{b,c,g,h}$) of both cells are not detectable, and may degrade the timing performance of the circuit. Therefore, these faults should be detected by means of alternate techniques such as I_{DDQ} testing [12].

Similar considerations hold for the detection of bridging faults, that have been reported to be the most common kind of failures in CMOS ICs [13]. The detectability of these faults has been studied by means of electrical level simulations, considering a bridging resistance of 100Ω . The results achieved have shown that 75% of the possible bridging faults can be detected in a conventional way, while the fault coverage grows to 89% if I_{DDQ} is used.

Some bridging faults, in fact, such as that between y_1 and y_2 , cannot be detected with the considered sequence (because they require that Φ_1 and Φ_2 are on-

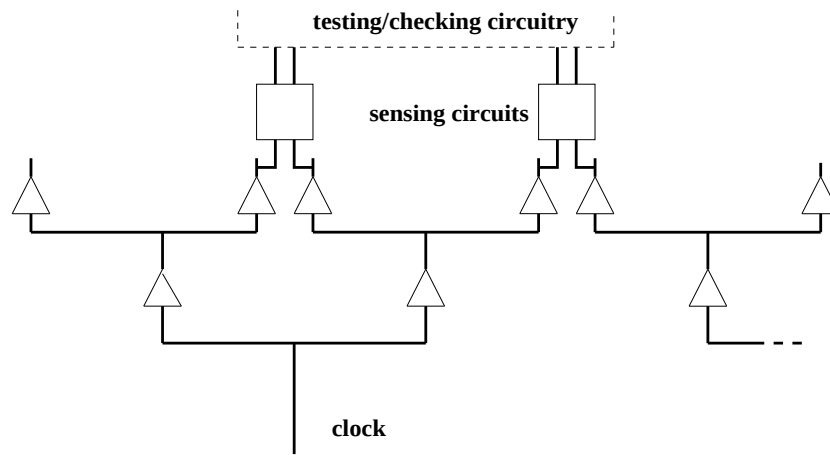


Figure 6: Schematic example of the possible use of the proposed sensing circuit inside a CMOS circuit to test the correctness of the clock distribution.

trolled to different logic values) and their occurrence probability should be reduced by acting at the layout level [14].

4 Conclusions

This work presents a new sensing circuit to be used in the detection of skews affecting the clock signal of synchronous systems. This problem, not yet addressed in the literature, is becoming critical with the increasing speed of digital circuits. This simple circuit can be used to monitor critical couples of clock wires inside the circuit in both off-line and on-line testing applications. The sensitivity and the testability of the proposed circuit have been analyzed, showing the effectiveness of the presented scheme.

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