Reconfigurable Data Converter as a Building Block for Mixed-Signal Test

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Abstract

A reconfigurable data converter (RDC) that can be configured to a number of ADCs and DACs having different speeds and resolutions for testing mixed-signal systems is proposed. It can be used as a building block in mixed-signal boundary scan or built-in self test (BIST) techniques. The RDC can also be configured as random noise generators and used as test stimuli in BIST. Since the required area of the proposed RDC is only slightly larger than that of a conventional pipelined ADC, it can be used in many mixed-signal systems.

1 Introduction

Recently, several design-for-test techniques (DFT) for mixed-signal systems have been proposed. These techniques utilize analog test buses [1] [2] [3], mixed-mode boundary scan [4] [5] and built-in self test (BIST) [6]. These techniques except those that use analog test buses usually require ADCs and DACs, which are assumed to be avaliable in very large mixed-signal systems. However, many mixed-signal systems contain either ADCs or DACs but not both. Incorporating additional data converters for DFT requires high area overhead. Furthermore, the conversion rate and the accuracy of the ADCs and DACs have to be high for high speed or high precision analog parts. In this paper, a high speed DFT building block called reconfigurable data converter (RDC) is proposed. This building block can be configured to different numbers of ADCs and DACs having different speeds and resolutions. The proposed RDC only requires an area slightly larger than a conventional pipelined ADC. Therefore, the area overhead for mixed-signal DFTs that use ADCs and DACs is greatly reduced. In addition, the RDC can be configured as analog random voltage generators and used as test-stimulus generators in mixed-signal BIST.

2 Reconfigurable Data Converter

The general structure of the proposed RDC is shown in Figure 1. It consists of an array of identical conversion stages (CSs) and an interconnection network (ICN). Each CS contains an amplifier, a k-bit flash ADC and a k-bit DAC. The flash ADC input and the amplifier input are selected by the multiplexer which is controlled by the signal S_i. The function of the CS is determined by the signal F_i. When F_i is set to 1, the CS is configured as a pipelined ADC stage.

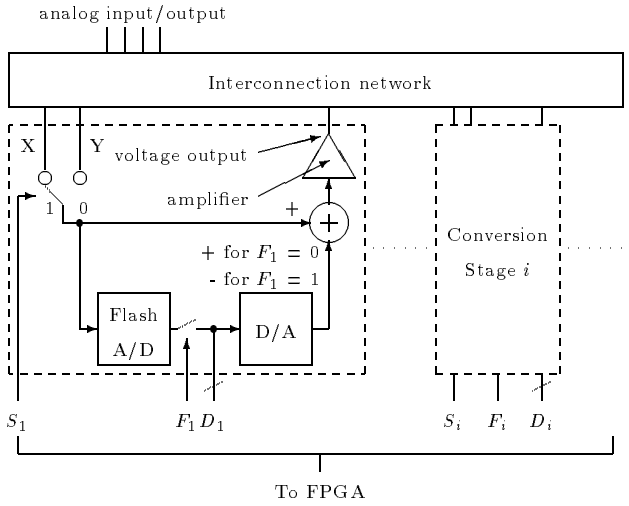

Figure 1: Reconfigurable data converter architecture

The gain of the amplifier is set to 2^k. The output voltage of the k-bit DAC is determined by the digital output D_i from the flash ADC. When F_i is set to 0, the CS is configured as a pipelined DAC stage. The gain of the amplifier is set to 2^{-k}. The k-bit DAC is controlled by digital input D_i. In the simplest case, the ADC and the DAC in each CS have 1-bit resolution and the gain of the amplifier is either equal to 2 or 1/2. This simple 1-bit CS can be realized using switched-capacitor techniques as shown in Figure 2. It can be configured to different configurations given in Table 1. Noted that the 1-bit CS can also be configured as a S/H circuit as indicated in the table. The configuration of the CS is controlled using additional logic circuits, for example, the test controller in BIST. The two non-overlapping clocks ϕ_1 and ϕ_2 are connected to the switches differently for odd and even CSs as indicated in Figure 2. Hence, the outputs of the odd and even stages are only valid at ϕ_2 and ϕ_1, respectively.

The proposed 1-bit CS allows the two capacitors and the opamp to be used for addition, subtraction, S/H operation, and amplification with a gain of 2 or 1/2. In comparsion to the conventional pipelined

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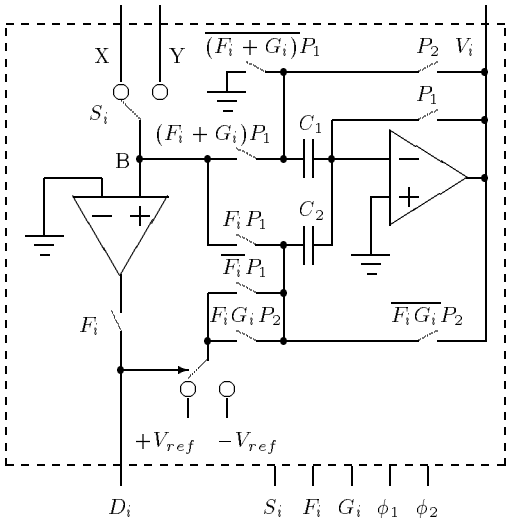

Figure 2: 1-bit CS ($P_1 = \phi_1$ & $P_2 = \phi_2$ for odd stages and $P_1 = \phi_2$ & $P_2 = \phi_1$ for even stages)

F_i	G_i	Configuration
0	0	DAC stage (with input set to zero)
0	1	DAC stage (normal)
1	0	S/H stage
1	1	ADC stage

Table 1: Configurations of the ith 1-bit CS

ADC, the proposed RDC design requires the same numbers of capacitors, opamps, and comparators and a few more logic gates. Hence, the RDC requires an area that is approximately the same as the pipelined ADC.

The design of an ICN for a RDC with 8 CSs is shown in Figure 3. The ICN allows the CSs to be connected to different groups. It also allows the outputs of the CSs to be fed as inputs to other CSs. Different data converters having different resoultions can be configured using different ICN connection (to be discussed in the next section). Since the number of switches between any two terminals is equal to one, the delay between CSs is minimized, and high speed operation can be achieved. The area requirment of the ICN is usually very small since there are only a few ways in which a wire can be connected.

3 Reconfiguration examples

The reconfigurability of the proposed RDC are demonstrated using different examples. If an N-bit ADC is required and M number of 1-bit CSs are avaliable where M is greater than or equal to $N+1$, the first CS is configured as a S/H circuit with the terminal X being the analog input and the remaining N CSs configured as ADC stages. The output of each CS is connected to the terminal Y of the next CS via the ICN. The digital outputs, D_1 and D_N, represent the

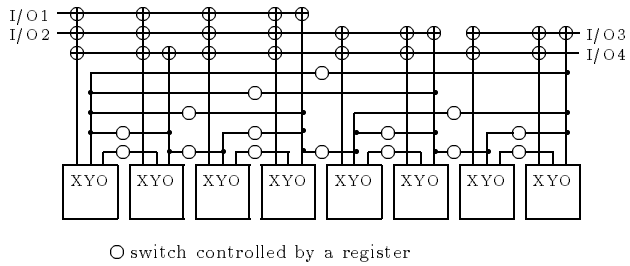

Figure 3: Interconnection network for 8 CSs

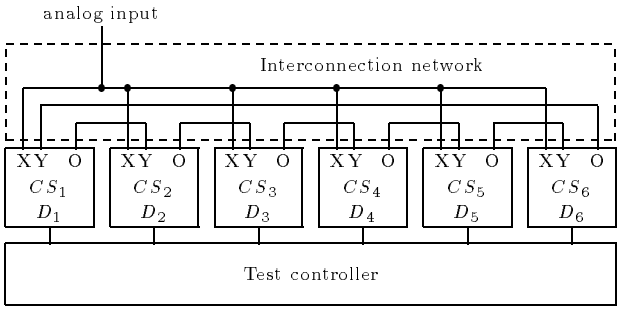

Figure 4: An 8-bit ADC realized in an RDC with 6 CSs

MSB and the LSB, respectively. Although it requires M clock periods to complete the conversion of one sample, the throughput is equal to 1 sample/clock period, and this is due to the use of pipelined structure. If an N-bit DAC is required, the first CS is configured as a DAC stage with the amplifier input set to zero and the remaining CSs configured as normal DAC stages. In this case, D_1 and D_N represent the LSB and the MSB, respectively. Since each CS can be reconfigured dynamically, the proposed RDC is also capable of implementing an ADC or an DAC with $N \geq M$. The configuration and the timing diagram of the RDC with $N = 8$ and $M = 6$ are given in Figures 4 and 5, respectively. Since M is equal to 6, the complete 8-bit output is obtained by feeding the output voltage of stage 6 back to the terminal Y of the first stage via the ICN. The analog input is sampled by generating the appropriate control signals, S_i, F_i and G_i for each CS from the test controller at each ϕ_1 and ϕ_2 to reconfigure the CSs into S/H circuits. The throughput for the example shown in Figure 4 is equal to 2/3 sample/clock periods. In general, if we assume that only L CSs are avaliable to realize an N-bit ADC, the throughput is equal to $2 \cdot \left\lfloor \frac{2N}{L} + 1 \right\rfloor^{-1}$ where L must be an even number and this is due to different connections of ϕ_1 and ϕ_2 for even and odd stages. Similarly, a DAC with $N > M$ can also be implemented by feeding the output voltage of the last CS back to the first CS. If multiple ADCs and DACs having different speed and resolutions are required, the CSs can be connected via the ICN to different groups. Since the clock phases

Clock Period		Conversion Stage					
		1	2	3	4	5	6
1	ϕ_1						
	ϕ_2	H1					
2	ϕ_1		11				
	ϕ_2			12			
3	ϕ_1		H2		13		
	ϕ_2			21		14	
4	ϕ_1				22		15
	ϕ_2	16		H3		23	
5	ϕ_1		17		31		24
	ϕ_2	25		18		32	
.				.			
.				.			
.				.			

Figure 5: Timing diagram for an 8-bit ADC realized in an RDC with 6 CSs ("Hi" represents holding the ith sample and "ij" represents the generation of the jth bit of the ith sample.)

between odd and even CSs are different, all the reconfigured ADCs or DACs must contain even numbers of CSs to ensure correct operation. More CSs can be allocated to the converters that require high speeds and resolutions. Furthermore, if high accuracy ADCs are required, fully-digitally self-calibration techniques can be used [7].

4 Mixed-signal boundary scan using RDC

In mixed-signal boundary scan, the digitized outputs of analog input peripheral circuits can be observed at the external pins via the boundary scan shift register. The digitized analog input to the analog output peripheral circuits can also be provided via the boundary scan shift register. Therefore, both controllability and observability for testing the analog circuits are provided. However, both ADCs and DACs are required to be connected to the boundary scan shift register. In some mixed-signal systems where there is only one ADC or one DAC, additional data converters have to be added for DFT, and therefore, the area overhead may not be acceptable. The overhead can be greatly reduced with the proposed RDC. Figure 6 illustrates the use of RDC in boundary-scan techniques. In this example, the RDC is assumed to function as an ADC during normal operation. When the system is in the test mode, the analog circuit connected to the primary input is digitized by the RDC and the digitzed output can be observed via the boundary scan shift register. To test the analog circuits connected to the primary output, the switch is turned to the T position. The RDC is then reconfigured as a DAC and the digitized analog input is applied to the RDC through the boundary scan shift register. If a number of nodes are required to be tested simultaneously, the RDC can be reconfigured to a number of different ADCs and/or

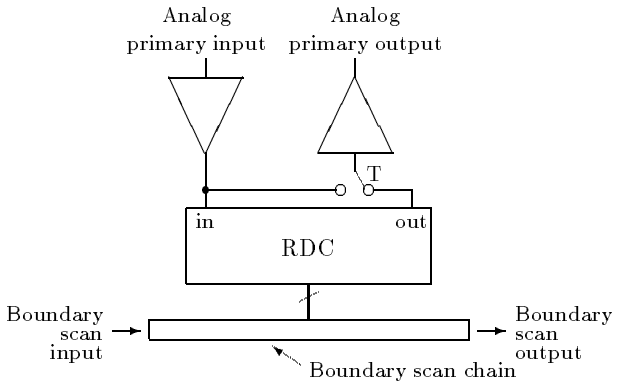

Figure 6: Mixed-signal boundary scan using RDC

DACs connecting to these nodes. Since only one RDC is used in place of several data converters, the area overhead for DFT is greatly reduced. However, the throughput of each converter in this case is lower than the throughput during the normal operation.

5 Mixed-signal BIST using RDC

In mixed-signal BIST, a test-stimulus generator and a test-response evaluator are required. The test-stimulus generator usually consists of a linear feedback shift register for generating a random digital sequence, and an DAC for converting the digital sequence into analog voltage [6]. The analog output signals for the device under test are converted to digital signals using an ADC. These digitized signals are then evaluated using a built-in logic block (BILBO) [6] or a DSP [8]. Similar to the boundary scan technique discussed above, the RDC can be reconfigured as a number of ADCs and DACs to perform data conversions required in the BIST. The area overhead again is reduced. In addition, the RDC itself can also be reconfigured to a random voltage generator as discussed below, and hence, linear feedback shift register is not needed.

To use the RDC as a noise generator, a simple technique called quantization noise regeneration is proposed [9]. The proposed technique is based on applying a feedback between the output and the input of a CS (configured as ADC stage) as shown in Figure 7. If the output of the CS e_n is assumed to be white and independent of the input signal u_n, it can be used to generate the next noise output signal e_{n+1}. If a delay within the CS is assumed, this concept can be represented using the block diagram shown in Figure 8 where the amplifier input ϵ_n represents the quantization error. In practice, the assumption that e_n is independent of u_n is invalid, and hence, the output e_n is not white.

To determine the statistical properties of the noise output e_n, the quantization error ϵ_n is normalized by a factor of $2V_{ref}$ as

$$\epsilon_n = \begin{cases} \frac{u_n}{2V_{ref}} - \frac{1}{2} & \text{if } u_n > 0 \\ \frac{u_n}{2V_{ref}} + \frac{1}{2} & \text{if } u_n < 0 \end{cases} \quad (1)$$

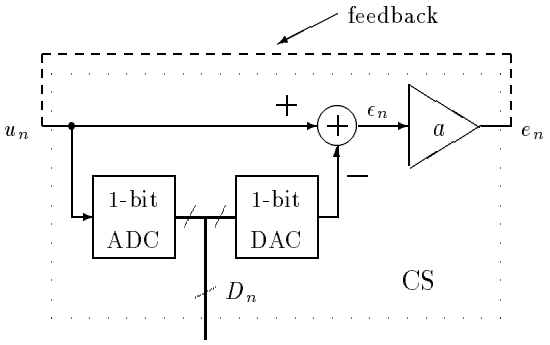

Figure 7: A CS (configured as ADC stage) with feedback

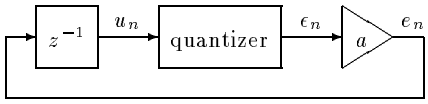

Figure 8: Block diagram representation of the quantization noise regeneration technique

The amplifier gain also has to be normalized to $2V_{ref}a$. Hence, e_n is equal to $2V_{ref}a\epsilon_n$. If u_n is bound between $-2V_{ref}$ and $2V_{ref}$, (1) can be rewritten as

$$\begin{aligned}\epsilon_n &= \frac{u_n}{2V_{ref}} - \left\lfloor \frac{u_n}{2V_{ref}} \right\rfloor - \frac{1}{2} = \left\langle \frac{u_n}{2V_{ref}} \right\rangle - \frac{1}{2} \\ &= \left\langle \frac{e_{n-1}}{2V_{ref}} \right\rangle - \frac{1}{2} = \langle a\epsilon_{n-1} \rangle - \frac{1}{2} \end{aligned} \quad (2)$$

where $\langle x \rangle$ represents the fractional component of x. One can also write the Fourier series for ϵ_n and ${\epsilon_n}^2$ [10] as

$$\epsilon_n = \sum_{l=1}^{\infty} \frac{1}{\pi l} \sin\left(2\pi l \frac{u_n}{2V_{ref}}\right) = \sum_{l\neq 0} \frac{1}{2\pi jl} e^{2\pi jl\frac{u_n}{2V_{ref}}} \quad (3)$$

$${\epsilon_n}^2 = \frac{1}{12} + \sum_{l\neq 0} \frac{1}{2(\pi jl)^2} e^{2\pi jl\frac{u_n}{2V_{ref}}} \quad (4)$$

From (3) and (4), the mean value and the second moment of e_n can be expressed as

$$\overline{E}\{e_n\} = 2V_{ref}a \sum_{l\neq 0} \frac{1}{2\pi jl} \lim_{N\to\infty} \frac{1}{N} \sum_{n=1}^{N} e^{2\pi jl\frac{u_n}{2V_{ref}}} \quad (5)$$

$$\begin{aligned}\overline{E}\{{e_n}^2\} &= 4(V_{ref}a)^2 \left(\frac{1}{12} + \sum_{l\neq 0} \frac{1}{2(\pi jl)^2} \times \right. \\ &\left. \lim_{N\to\infty} \frac{1}{N} \sum_{n=1}^{N} e^{2\pi jl\frac{u_n}{2V_{ref}}} \right) \end{aligned} \quad (6)$$

where $\frac{u_n}{2V_{ref}} = \frac{e_{n-1}}{2V_{ref}} = a\epsilon_{n-1}$. Using the fact that $e^{2\pi j\langle x\rangle} = e^{2\pi jx}$, the term $e^{2\pi jla\epsilon_{n-1}}$ can be expressed as

$$e^{2\pi jla\epsilon_{n-1}} = e^{2\pi jl\langle c(n)\rangle} \quad (7)$$

where $c(n) = a^n\epsilon_0 - \frac{1}{2}\frac{1-a^n}{1-a} + \frac{1}{2}$. Note that

$$a^n = e^{n\ln a} = 1 + n\ln a + \frac{(n\ln a)^2}{2!} + \cdots$$

Then the limits in (5) and (6) can be evaluated using the general version of Weyl's theorem (see example in [10]): If

$$b(n) = a_0 + a_1 n + a_2 n^2 + a_3 n^3 + \cdots \quad (8)$$

where a_is are real coefficients and if at least one of the coefficients is irrational for $i \geq 1$, then

$$\lim_{N\to\infty} \sum_{n=1}^{N} g(\langle b(n)\rangle) = \int_0^1 g(y)dy \quad (9)$$

where $g(y)$ is any integrable functions. Since $c(n)$ in (7) has the same form as that in (8), the limits in (5) and (6) are equal to 0 for $l \neq 0$ and 1 for $l = 0$. Therefore, the mean and variance of e_n are found to be 0 and $\frac{(V_{ref}a)^2}{3}$, respectively. Furthermore, the auto-correlation between e_n and e_{n+k} can also be derived based on (3) and (7).

$$\begin{aligned}\overline{E}\{e_n e_{n+k}\} &= \sum_{l\neq 0}\sum_{i\neq 0} \frac{-4(V_{ref}a)^2}{4\pi^2 li} e^{2\pi j\frac{ai}{2}(1-\frac{1-a^k}{1-a})} \times \\ &\lim_{N\to\infty} \frac{1}{N} \sum_{n=1}^{N} e^{2\pi ja(l+ia^k)\epsilon_{n-1}} \end{aligned}$$

Using (9), the limit in the above equation is equal to 0 for $l \neq -ia^k$ and 1 for $l = -ia^k$. Let $\beta = \frac{a}{2}(1-\frac{1-a^k}{1-a})$, the auto-correlation can be derived as

$$\overline{E}\{e_n e_{n+k}\} = \frac{4(V_{ref}a)^2}{a^k}\left[\frac{1}{12} - \frac{\langle\beta\rangle(1-\langle\beta\rangle)}{2}\right] \quad (10)$$

Based on (10), $\overline{E}\{e_n e_{n+k}\}$ is not zero, and hence, the output is not white. However, $\overline{E}\{e_n e_{n+k}\}$ exhibits an exponential decay towards zero for large k. Compared to the noise generation using a linear feedback shift register, the auto-correlation does not repeat but has a higher correlation between adjacent samples. This correlation can be alleviated if the output is taken at every time interval of k such that $\overline{E}\{e_n e_{n+k}\}$ falls within an acceptable level. However, the throughput will be reduced by $\frac{1}{k}$. To increase the throughput, N number of CSs can be connected in cascade and the output of the last CS is fed back to the first CS as shown in Figure 9. If the initial voltage of each CS is

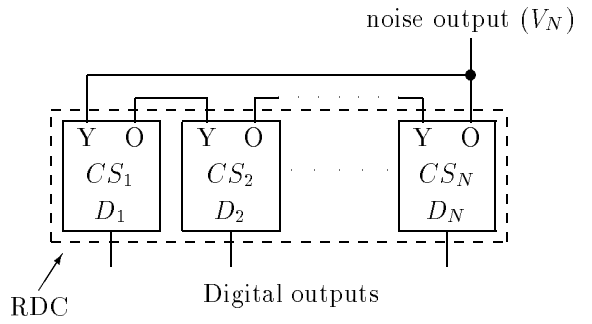

Figure 9: RDC configured as an noise generator

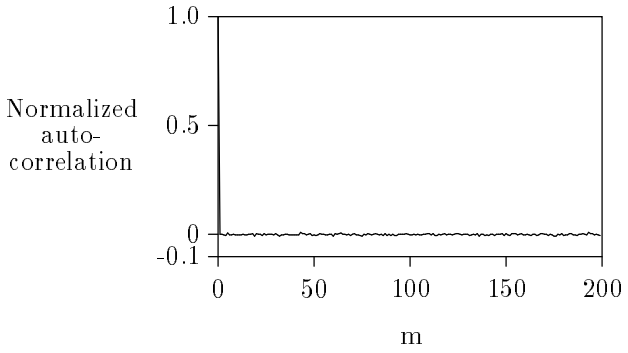

Figure 10: Estimation of auto-correlation of V_N

set independently, there will be no correlation within a window of N samples but the correlation between e_n and e_{n+kN} is proportional to $\frac{4(V_{ref}a)^2}{a^{kN}}$ which is very small. Therefore, the output V_N can be considered as a uniformly distributed white noise. In practical situations, V_N may settle to a DC voltage [9] if the amplifier gain a in each stage is exactly equal to two. This problem can be solved if the gain in any one of the N stages is slightly less than 2 [9].

To simulate the proposed noise generator, a computer program was written for an RDC with 8 CSs. V_{ref} and $-V_{ref}$ were set to 1 and -1, respectively. Therefore, the input range was limited to values between -1 and 1. The amplifier gain for the last CS was set to 1.999 and the amplifier gain for other CSs was set to 2. The normalized auto-correlation of V_N was estimated using 100k samples with a correlation estimation length of 200. The result is shown in Figure 10. The correlation ranges between 0.0097 and -0.0078 for $m > 0$. The mean and variance are 0.00215 and 0.332, respectively. These values are very closed to those of ideal uniform distribution (mean = 0 and variance = 1/3). Therefore, V_N can be considered to be a random signal uniformly distributed between $+V_{ref}$ and $-V_{ref}$. Since each sample (V_N) is quantized by the RDC to produce the next sample, the digitized V_N from the digital outputs of the RDC is also avaliable to the test evaluator.

6 Summary and conclusion

A pipelined RDC architecture for mixed-signal DFT is proposed. Different numbers of ADCs and DACs having different throughputs and resolutions can be realized. The throughputs of the configured converters depend on the numbers of CSs used in individual converters and their required resolutions. Since the RDC can be reconfigured to a number of different ADCs and/or DACs, the area overhead for mixed-signal boundary scan or BIST can be greatly reduced, especially if the system under test requires only one data converter during normal operations. The RDC can also be configured as random signal generators used as test stimuli in BIST. The generated random signals are also available in digital form, enabling the digital test evaluator to compare and evaluate the inputs and the outputs of the system under test. Since the area requirement of the RDC is about the same as a conventional pipelined ADC, the RDC can be used as a building block for mixed-signal DFT with low area overhead.

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