

A Production-oriented Measurement Method for Fast and Exhaustive Iddq Tests

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Abstract

The paper describes a measurement method to perform an iddq test on each vector of a test pattern. The measurement is performed using the functional test mode of a digital tester. Vector rates between 100KHz and 10MHz yield a current resolution of 10uA to 100uA. The great advantage of the method is that the measurements are performed by using only the tester's pin electronic and the existing control software. No additional equipment is necessary and the setup of the loadboard is made without any additional components except a buffering capacitance for the device, if needed. The application of the method to the iddq test of an 8 bit microcontroller is described.

Introduction

Since Iddq testing appeared in the literature the first time, a lot of research has been done and published [1-5]. In the meantime there is no doubt anymore that iddq testing is a very powerful method to increase the number of detectable technological defects and to localize design oriented problems. Less vectors are needed to achieve the same or even a better fault coverage [9]. Various studies have been performed showing clearly that the quality of the devices could be improved after introduction of iddq testing. Nevertheless, it is still an unsolved problem how iddq measurements can be performed in order to make the test suitable for the production environment.

Two principal measurement methods exist [6,9]. One method uses a current meter in the supply path, which is bypassed by a relais or a FET during the switching phase. The other method uses a relais or FET to disconnect the power pin from the device after the switching process is completed. Then the voltage decay at the power pin due to leakage is measured. Mostly, the device is stimulated by a vector sequence to reach a certain state, then the device clock is stopped holding the input data and the measurement is performed by a dc parametric measurement unit.

When implementing such a method, two major problems occur. On the one hand, standard dc measurement equipment is very slow in speed, especially when very small leakage currents have to be detected. Therefore, in current approaches, iddq is measured only for a few specific vectors. On the other hand, a special configuration on the loadboard containing a bypass circuitry for the current peaks has to be provided. In this respect, it has to be taken into account that the supply current is a high frequency signal with a bandwidth of several GHz and a dynamic in the amplitude of about 10^6 or more. Therefore, the practical implementation of the auxiliary circuitry on the loadboard needs special care.

These practical problems led to the idea to make use of the high speed switching and measurement capability of the tester's pin electronic also for the power supply of the DUT. Thus, the existing infrastructure on the tester could also be used for configuring an iddq test with a minimal effort but high performance.

The Basic Idea

The basic idea of the measurement method is to use one or more driver channels of the tester as a ground supply for the device. One of the channels is configured as an io-channel in order to monitor the voltage at the Vss pin of the device with the receiver part of the pin electronic (fig1).

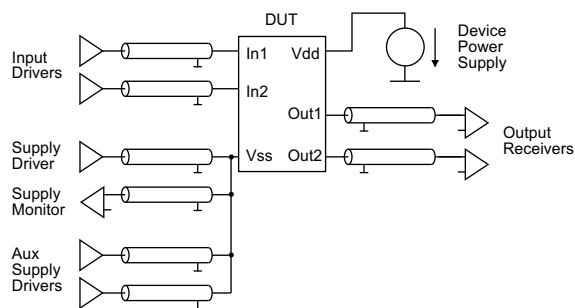


Fig. 1: DUT connection to the tester

During the switching of the device, the ground supply channels force a fixed zero voltage and after the dynamic current has decayed to the quasistatic leakage current, the supply channels are switched to the high impedance state (fig. 2).

There is one important reason, why Vss is monitored for Iddq testing. When a pin driver is used as power supply to a circuit, it may still be desirable to monitor the functionality of the circuit at the outputs of the device simultaneously by means of normally used receivers. This ensures that Iddq testing is performed under conditions that will also result in a functional pass. Since the input resistance of the receivers at the outputs of the device is several kOhm to ground, a leakage current flows through the Vdd pin of the device but not through the Vss pin, which is monitored. Hence, the Iddq result is not influenced by the receiver leakage.

For p-well technologies there is another reason. It is often desirable to exclude the pads from the Iddq test of the core logic. This may be necessary, if pull-up or pull-down pads are used producing a constantly high leakage, or if bidirectional pads are used, and the tester load cannot be switched off during Iddq testing. If a p-well technology is used, Vss is connected to the p-well areas, while Vdd is connected to the common substrate. Normally the pads use a well area which is separated from the well area of the core logic. In this case only the core Vss supply is forced and monitored by tester channels, while Vss of the pads remains connected directly to system ground. Of course, if a n-well technology is used, Vdd has to be forced by tester channels in order to restrict the Iddq test to the core area.

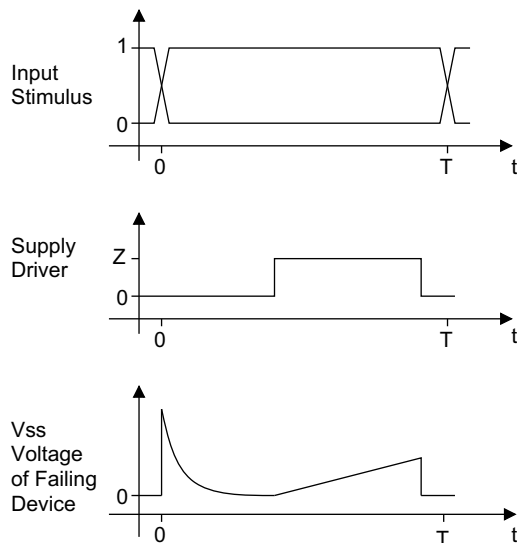


Fig. 2: Timing of the supply driver

Since one of the supply channels is configured as bidirectional and the driver part is in the high impedance state, only the input impedance of the receiver part is connected to the Vss pin of the device. If the device has an abnormal leakage current, the voltage at the Vss pin will increase with a time constant given by the leakage current and the capacitance at the Vss pin. The receiver compares the voltage with the expected zero voltage at the end of the high impedance state and detects the leakage. Before starting with the next tester cycle, the pin drivers are switched back to force the Vss voltage.

State-of-the-art testers use matched transmission lines to connect the pin electronics with the device pins. Since the switching of the device produces current peaks in the range of nanoseconds, the power connection has to be treated with respect to transmission line theory.

During the switching of the device the supply channels force the Vss voltage with the driver impedance of 50 Ohm (depending on the tester type) via transmission lines into a very low impedance of the device Vss. Current and voltage waves get reflected back into each transmission line and are absorbed totally at the matched driver side. Therefore, the temporal behaviour of the voltage at the Vss pin of the device can be seen after the propagation delay without any further reflections. After the switching current has decayed to zero, the Vss pin of the device, the transmission lines and the pin electronics of the tester are discharged to zero volts. Under these conditions the pin electronic may switch the driver to high impedance without introducing a change of charge into the transmission line.

A Model for Resistive Power Supply

When driver channels are used in order to supply either ground or Vdd, a voltage drop at the drivers internal resistance occurs whenever the device sinks current. This happens mainly, when the circuit is switching as a reaction upon a change of input stimulus. This voltage drop has to be controlled exactly to guarantee the functionality of the device. For a device connected to a voltage controlled power supply, which is buffered with additional capacitances directly at the power pins, the switching times of internal gates are below 1ns. Therefore, very short current peaks are generated. The current peaks of all gates switching simultaneously accumulate to a strong and short current supply peak, only limited by inductances in the supply path.

In this respect in some literature it is stated that if the saturation current of a single transistor in a state-of-the-art technology is several milliamps, and if only some percent of the gates of a large and complex device with more than 1 million transistors switch simultaneously, inserting a shunt with several ohms would cause a voltage drop that is larger than the supply voltage. Or, in other words, the device would

not work anymore. This coarse consideration is wrong because it omits some important technological details which will be considered in the following.

To describe the behaviour of the supply current analytically, a simple model for a CMOS circuit is developed. As a starting point for the model, the voltage at a shunt inserted in the supply path of several large devices was investigated with an oscilloscope at high temporal resolution. First of all, it was found that all devices passed the functional test even if a large shunt was inserted. However, the tester cycle time has to be increased significantly to obtain a pass. Fig. 3a shows a section of the current signal for the IMS PRIMO5 device (2.7 k active transistors) operated at 2 MHz vector rate. The signal is taken as a voltage at a 50 Ohm shunt for about 1.4k of stimulus pattern. Fig 3b shows a zoom into the signal for 10 vectors. The traces show a steep rising edge and an exponential decay of the peaks. This behaviour is typical for all chips investigated.

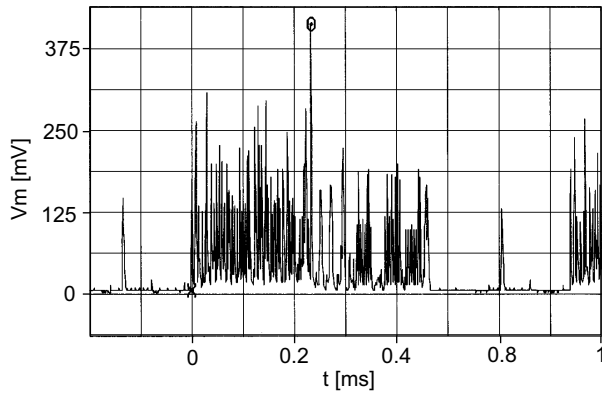


Fig. 3a: Supply current signal for the PRIMO5 device

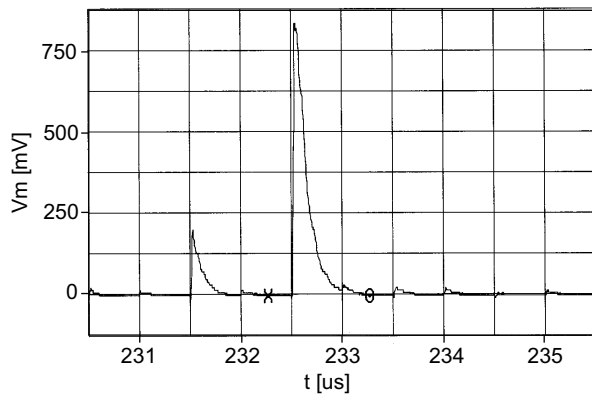


Fig. 3b: Detail of the PRIMO5 supply current signal

The experimental result gives an indication that charging and discharging can be modelled by using a simple RC model.

This model was developed for a basic inverter cell. Fig. 4 shows a cross-section through the technological implementation of an inverter. The capacitances which have to be charged in the case of an inverter are the drain capacitances of the NMOS and the PMOS transistor, and the load capacitance attached to the output. The load capacitance consists of the gates driven and the capacitance of the interconnection lines.

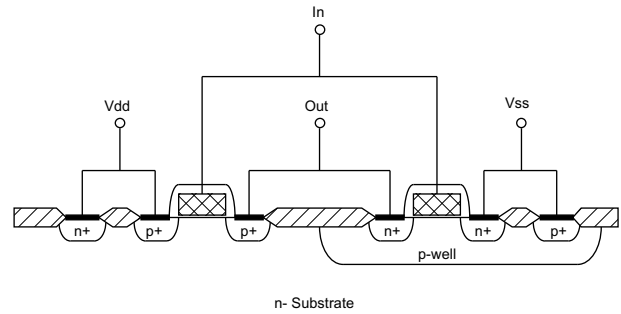


Fig. 4: Cross-section through a basic inverter cell

If the leakage of the transistor is neglected, the transistor can be modelled by an ideal switch with an on resistance R_d . The output capacitance is separated into a capacitance to ground and to V_{dd} , and they are assumed to be identical with the value C_d (fig. 5).

When the current is supplied from an ideal voltage source with zero resistance, the device-internal capacitance between V_{dd} and V_{ss} can be neglected because the power supply is able to provide the necessary charge instantly. This capacitance C_{dd} is mainly formed by the junction capacitance between the well and the substrate. Most of the CAD layout extraction tools do not extract this capacitance by default.

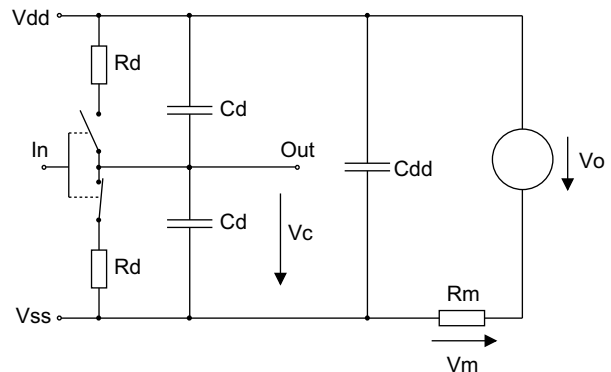


Fig. 5: RC model of the basic inverter cell

However, the capacitance C_{dd} plays an important role, when the voltage source has a significant internal resistance R_m .

Due to the design rules, the well area is much larger than the transistor area and is combined with other cells which do not switch. Even if the per area capacitance of the well is about one half of the respective value of a diffusion region, it is larger by far than the capacitance of the switched output node due to the much larger total area. It should be emphasized that this is independent of the circuit size.

The charge needed to switch the output node from low to high or vice versa is determined from $Q = C_d * V_{dd}$. This charge Q is represented by the area below the current peak. If the output switches, a voltage drops at R_m due to the charging current, but the more the voltage drops, the more charge will be taken immediately from C_{dd} . After switching, C_{dd} is charged to V_{dd} again, with a time constant of about $R_m * C_{dd}$. Normally, this constant is much larger than the time constant needed to charge C_d . Therefore, the capacitance C_{dd} buffers the peak size of the voltage drop. The peak visible at R_m represents the charging of C_{dd} rather than the charging of the switched internal nodes.

If R_m is increased, the time needed to refill the buffer increases, and the area below the peak is distributed over a longer time with a smaller current value at the maximum. As a consequence, the voltage drop at R_m approaches a limit, if R_m is increased to high values. The limit can easily be determined, assuming an infinite value for R_m . In this case C_d is completely charged from C_{dd} , and the final potential at C_d is given by:

$$V_c = V_o \frac{C_{dd}}{C_d + C_{dd}} \quad (1)$$

Therefore, the upper limit of the voltage drop at R_m will be:

$$V_{m\lim} = V_o \frac{C_d}{C_d + C_{dd}} \quad (2)$$

We also must take into account that for all gates which do not switch, the output capacitance is connected to either V_{dd} or V_{ss} through one or more transistors. This capacitance is also a contribution to the C_{dd} capacitance.

Since the model contains only two capacitances, it can be treated analytically by a second order differential equation. The voltage at C_d is given by:

$$a \frac{d^2 V_c}{dt^2} + b \frac{dV_c}{dt} + V_c = V_o \quad (3)$$

$$a = R_m C_{dd} R_d C_d \quad b = R_m C_{dd} + R_d C_d + R_m C_d$$

The solution of this equation is the superimposition of two

exponential functions:

$$\frac{V_c(t)}{V_o} = k_1 e^{-t/T_1} + k_2 e^{-t/T_2} \quad (4)$$

$$k_1 = \frac{T_1 T_2 - R_d C_d T_1}{R_d C_d (T_1 - T_2)} \quad k_2 = - \frac{T_1 T_2 - R_d C_d T_2}{R_d C_d (T_1 - T_2)}$$

$$T_{1/2} = \frac{2a}{b \pm \sqrt{b^2 - 4a}}$$

The voltage at R_m is given by:

$$\frac{V_m(t)}{V_o} = k_3 e^{-t/T_1} - k_3 e^{-t/T_2} \quad (5)$$

$$k_3 = - \frac{T_1 T_2 - (T_1 + T_2) R_d C_d + R_d^2 C_d^2}{R_d C_d (T_1 - T_2)}$$

Typically, $V_m(t)$ rises exponentially with a small time constant T_1 and decays again with a larger time constant T_2 . T_1 is mainly influenced by R_d and C_d while T_2 is dominated by R_m and C_{dd} . The maximum peak size of V_m can be calculated from:

$$\frac{V_{m\text{peak}}}{V_o} = k_3 \left(\frac{T_2}{T_1} \right)^{-T_2/(T_2-T_1)} - k_3 \left(\frac{T_2}{T_1} \right)^{-T_1/(T_2-T_1)} \quad (6)$$

Fig. 6 shows the behaviour of $V_{m\text{peak}}$ for different values of C_{dd} versus R_m . R_d was chosen to 50 Ohm, and C_d to 1nF. The peak limitation becomes much effective much faster, if C_{dd} is large. In this case the value of $V_{m\text{peak}}$ is small, which means the circuit is buffered more efficiently.

If for any case, the relation between the switched capacitance and the internal buffering capacitance is non-typical, e.g if the receiver load is not switched off, C_{dd} can be increased artificially by adding an external capacitance to C_{dd} . By this means, the voltage drop can be controlled not to increase excessively. However, this will also increase the time constant T_2 which determines the decay of the peak.

If the voltage drops temporarily, the functionality of a CMOS gate is not affected, since the switching threshold will always be half of the supply voltage. At the interface to the tester however, problems may occur. If the pad supply is included for I_{ddq} testing, and the voltage drop is more than about 0.7V, the esd protection diodes at the input pads may be forwardly biased, resulting in a current flow from the input drivers to V_{ss} or V_{dd} . If only the core logic is supplied by a resistive voltage supply, the logic levels of the core logic and the pads may be temporarily misadjusted. Therefore, the

voltage drop at the resistive supply has to be limited by an additional capacitance between Vdd and Vss in that case.

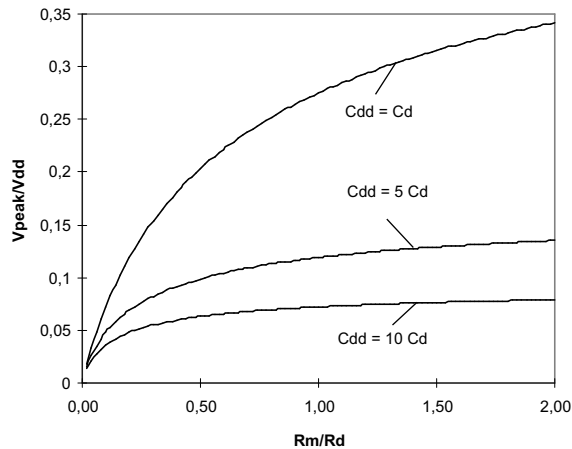


Fig. 6: Max. voltage drop at Rm for different values of Cdd

From the model description follows, that the time needed for the decay is determined mainly by the internal resistance of the driver. If the decay time appears to be too long for a single channel, more channels may be used in parallel. Nevertheless, this increases the capacitance at the supply pin. Therefore, the current detectable at the end of the high impedance phase is reduced. This agrees with the fact that cycle time and current resolution are always antagonists.

In a large and complex circuit switching may be a distributed process which lasts most of the cycle time. A good design however, uses a master clock for synchronization of all logic activity. Therefore, all switching will normally be concentrated near the clock edges. The experience with different circuits of different complexity showed that the superimposition of the current peaks of many gates may also be described by exponential functions, and the model may be used even for a whole circuit.

Application of the model

For the demonstration of the agreement between the analytical description and practical results on the tester the IMS UC11053 ASIC was used. This ASIC contains an 8 bit embedded microcontroller with 64*8 bit dual port ram and an universal asynchronous receiver and transmitter circuit. It is a 84 pin device measuring 6.5 * 6.5mm chip area, with a complexity of 27850 active transistors, fabricated on the IMS 1.2um GATE FOREST gate array (fig 7). Normally, the circuit is operated at 10 MHz. The test system used was a HP83000 digital test system.

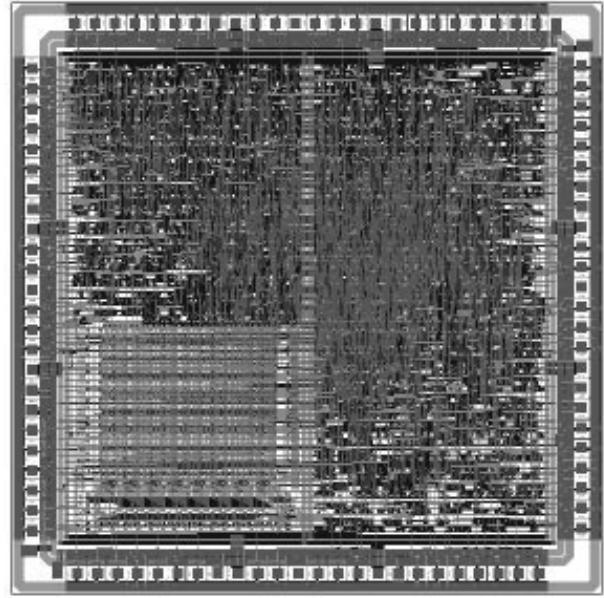


Fig. 7: The IMS UC11053 microcontroller

A 24k vector pattern was used as stimulus during the test. Since core and pad supply is separated, only the core logic was supplied by driver channels of the tester. The functionality of the circuit was monitored simultaneously by receivers connected to the device outputs.

In order to measure the superimposition of all peaks for all vectors, the expected data of the receiver part of the supply channel was set to logic low for all vectors. To measure the voltage drop in a quasi analogue way, a shmoo plot was performed. For obtaining this plot, the sampling point of the supply channel was swept in X-direction, and its low level was swept in the Y-direction while plotting the pass-fail result.

Several measurements with a different number of supply driver channels were performed to show the dependency on the internal resistance of the voltage supply. Fig. 8a-c shows the voltage drop at the supply monitor for 1 channel (50 Ohm), 2 channels (25 Ohm) and 4 channels (12.5 Ohm internal resistance). It becomes obvious that the voltage drop decreases by a factor of about 0.8 per channel. The decay time however, decreases nearly proportionally (see also fig. 6).

From these measurements it becomes evident, that increasing the shunt, the maximum voltage drop approaches a limit and the decay increases proportionally as predicted by the model.

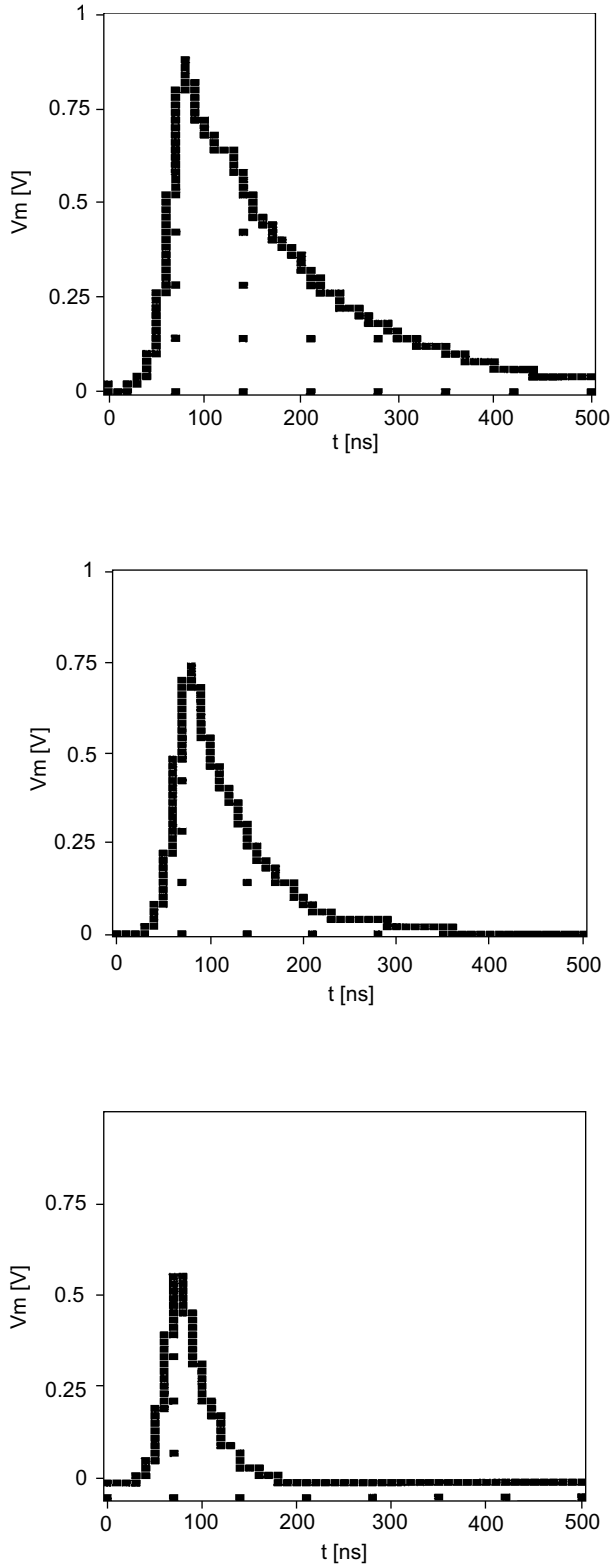


Fig. 8a-c: Voltage drop for different values of R_m ,
a) $R_m = 50 \text{ Ohm}$, b) $R_m = 25 \text{ Ohm}$ c) $R_m = 12.5 \text{ Ohm}$

Setup of the iddq measurement

When the current peak has decayed to the leakage current, the pin driver of the supply channel may be switched off. Since the timing is set up globally for each vector cycle, the leakage current condition has to be reached for all vectors. Depending on the tester type, there are various possibilities to switch a driver pin to high impedance. A very universal approach is to insert a new vector for each existing vector, which repeats the existing data but contains the high impedance information for the supply channel. A more sophisticated way is possible for testers which allow the composition of timing formats with respect to timing edges. Fig. 9 shows a drive format, which first drives a fixed logic zero and then switches to high impedance. At the end of the tester cycle, the driver is forced to drive a fixed zero again. In this case, no data have to be stored in the vector memory for the driver part. The receiver is set up to perform an edge compare to the contents of the expected data memory at the end of the high impedance phase. Normally, the expected data is a fixed zero which uses the low level parameter as the iddq threshold. Nevertheless, it may be necessary to mask vectors from being iddq tested.

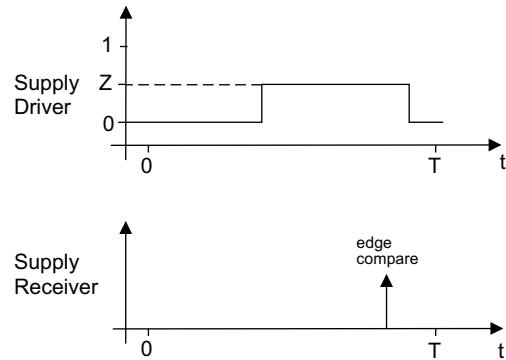


Fig. 9: Timing of the supply monitor channel

When the driver is in high impedance state, the V_{ss} pin will be charged towards V_{dd} by the leakage current. The voltage value reached for a given abnormal leakage current, in comparison with the normal leakage, represents the iddq sensitivity. The time constant for this charging process depends on the capacitance at the V_{ss} pin and the leakage current. The voltage behaviour during the high impedance phase is therefore described by the simple relation:

$$\frac{du}{dt} = \frac{i(t)}{C_{dd}} \quad (7)$$

For some testers the input resistance of the receiver is below 100 kOhm and cannot be neglected. It acts like a pulldown and reduces the iddq sensitivity.

Fig. 10a,b shows the voltage monitored at Vss of the UC11053 device. Vss was supplied by 4 channels, switched to high impedance between 300 and 900ns with respect to a tester cycle of 1000ns. Fig. 10a shows the charging behaviour with no abnormal leakage current, fig. 10b shows the conditions for an extra leakage of 500 μ A. Most of the testers offer a linear or binary search algorithm for finding a pass fail transition for the variation of given timing or level parameter. This may be used for defining the correct iddq threshold, if it is applied to the receiver's low level. For the UC11053 device we obtained the following values using a compare strobe at 800ns (see also fig. 11):

additional leakage	min low level for a pass
1mA	312mV
500 μ A	202mV
100 μ A	116mV
50 μ A	108mV
0	100mV

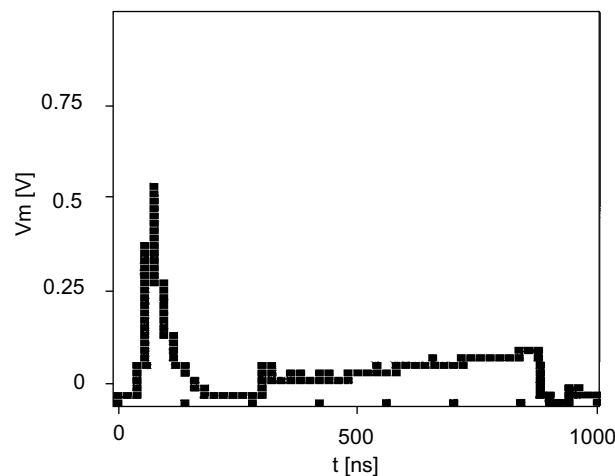


Fig. 10a: Monitor Signal, no extra leakage

As a result, this setup is sufficient to perform an iddq test at 1MHz with a leakage current resolution of 50 μ A. The whole vector set is tested in 24 μ s. The current resolution is about 2.5% of the maximum current of the smallest transistor and is therefore sufficient to detect the majority of possible defects.

The current sensitivity could be increased further, if the time the supply driver is set to tristate would be increased too. However, this would reduce the vector rate respectively. Therefore, it can be stated that the current sensitivity is not limited by the method but rather by the time granted for the measurement.

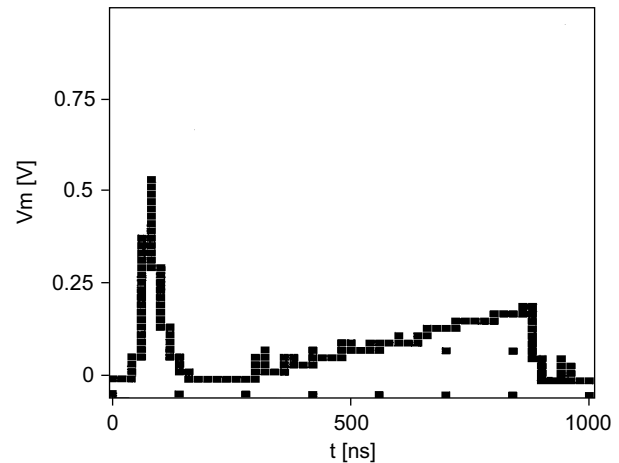


Fig. 10b: Monitor signal, 500 μ A extra leakage

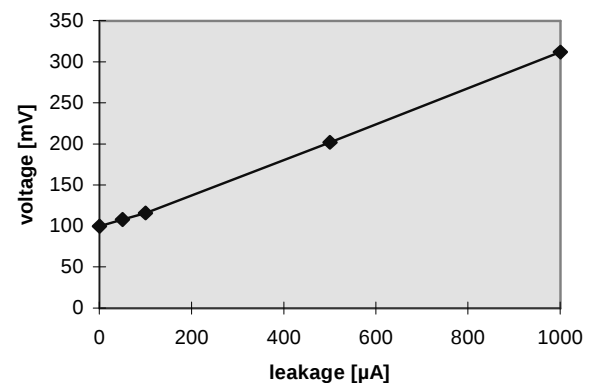


Fig. 11: Voltage drop versus leakage

Conclusion

Theoretical considerations and practical experience revealed that it is possible to use the pin driver capability of a tester to provide the power supply to a CMOS device. The voltage drop at the internal resistance is limited by default and may be monitored by means of standard testfunctions (e.g. a shmoo plot). If necessary, the peak maximum can be adjusted easily by an additional buffering capacitance between Vdd and Vss. Using the tristate capability of the supply channel in conjunction with the high speed compare capability of the receiver part, a very simple setup for iddq tests with high performance can be achieved. Loadboard configuration is reduced to a minimum, equal to standard

functional testing. No additional equipment is necessary and the complete infrastructure of the tester's control software can be used for iddq testing. The iddq setup was demonstrated for an IMS microcontroller ASIC, achieving a current resolution of 50uA and a vector rate of 1MHz.

Outlook

Achieving the goal of zero defects per device is desirable for systems containing many components. This is especially the case for multi chip modules (MCMs) or the chip on board (COB) technology. Since bare dice are used instead of packages, a high fault coverage has to be achieved already during wafer level tests. Porting the iddq measurement method to the wafer level seems to be well suited for that purpose. In addition, some problems as for example the separation of core and pad supply can be handled easier on the wafer level. Furthermore, the quantity of measured iddq mapped to the chip location on the wafer may be an important feedback for process control. Therefore, wafer level iddq tests will be subject to future investigations.

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