CCII+ Current Conveyor Based BIC Monitor for I_{DDQ} Testing of Complex CMOS Circuits

V. Stopjaková[1] and H. Manhaeve[2]

[1)] Department of Microelectronics, Slovak Technical University,
Ilkovicova 3, 812 19 Bratislava, Slovakia
Phone: +42 7 791 324
Fax: +42 7 723 480
E-mail: stopjak@elf.stuba.sk
[2)] Department of Microelectronics, KHBO,
Zeedijk 101, Oostende, Belgium
Phone: +32 59 508 996
Fax: +32 59 704 215
E-mail: manhaeve@kh.khbo.be

Abstract

In this paper, a quiescent built-in current (BIC) monitor based on a second generation current conveyor CCII+ is presented. The monitor circuit minimises the power supply voltage degradation and provides a sensitive detection of defects that cause an elevated value of the I_{DDQ} current. The proposed monitor offers an accurate current measurement and has a wide operation range. The CCII+ based current monitor is able to handle huge digital ASICs. Significant results summarising possibilities and limitations of the circuit are discussed as well. The design was implemented through Alcatel-Mietec 0.7µm CMOS technology and an evaluation of the prototype chips has been carried out. An experimental application of the proposed monitor in new analogue self-test structure was considered.

1 Introduction

It was found out that a number of realistic physical CMOS defects, such as gate-oxide shorts, bridges, opens and floating gates, are not detected by a conventional voltage based test approach. Quiescent power supply current testing [1]-[3], a test technique which is based upon the fact that defective circuits produce an abnormally high value of quiescent power supply (I_{DDQ}) current, has been proven to be very efficient in detecting certain defects occurring in CMOS ICs, requiring only a reduced number of test patterns [4]-[6]. Therefore, I_{DDQ} testing is very promising test method to increase quality and reliability of CMOS ICs in the field.

However, the implementation of this approach is not easy task and a dedicated measurement hardware is needed to perform I_{DDQ} testing. Since built-in current monitors are more sensitive and they can achieve much higher testing speeds than off-chip alternatives, they have been evaluated as an appropriate choice for CMOS VLSI current testing [7]. Consequently, a significant number of BIC monitors have been published [8]-[12] in the last couple of years. However, one serious drawback of BIC monitoring is that the area overhead demanded by the monitor is usually too large and only a few high-reliability applications find it practical.

In this paper, the development of a new on-chip current monitor is presented. The circuit, based on CCII+ current conveyor structure, is placed in the VDD power supply line of the device under test (DUT). The accuracy of the proposed BIC monitor is evaluated in the working range from 50nA to 600µA. The monitor circuit has been designed for I_{DDQ} testing of low voltage 3.3V CMOS ASICs. The technology selected is the Alcatel-Mietec 0.7µm CMOS, and a low silicon area overhead is achieved. The BIC monitor design was implemented into an analogue full custom design in order to prove its effectiveness also in analogue or mixed-signal testing. Finally, an experimental implementation of the monitor together with a complex low voltage digital CMOS ASIC is considered in the future.

ED&TC '97 on CD-ROM

The CCII+ current conveyor theory

In principle, the CCII+ circuit is a three-terminal device with two inputs X, Y and one output Z. In mathematical terms, the I/O characteristics of the CCII+ can be described by the following hybrid matrix:

$$\begin{bmatrix} i_y \\ V_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} V_y \\ i_x \\ V_z \end{bmatrix}$$

The voltage at the low impedance input node X follows the one present at the high impedance input node Y, while the input current at node X is mirrored to the high impedance output Z [13]-[14].

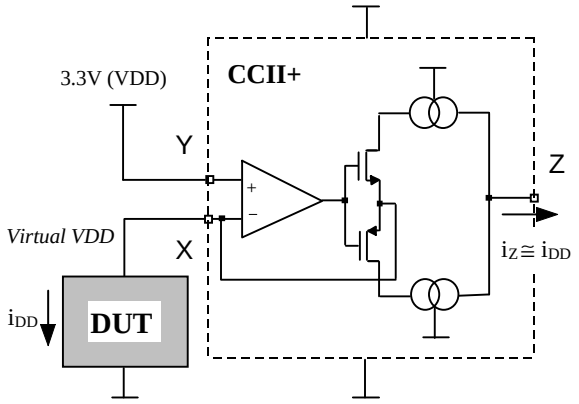

Figure 1 CCII+ arrangement for I_{DDQ} testing

It has been considered, that the CCII+ arranged with other circuits in a proper configuration might be very useful in I_{DDQ} testing of CMOS VLSI circuits (Figure 1). In the configuration mentioned above, the *Virtual VDD* at the node X follows the VDD power supply applied to the terminal Y, and the input current I_{DD} is mirrored to the output and consequently led to a current comparator. To stabilize the voltage at the terminal X (Virtual VDD) in a wide range of the input currents, an OpAmp-based current conveyor was designed. Furthermore, significant improvement in the accuracy of the current measurement (for the range of I_{DD} currents from 50nA to 600μA), is achieved by inserting regulated cascode mirrors into the CCII+. This structure provides precision current mirroring of the supply current.

2 The proposed monitor circuit

The proposed quiescent monitor circuit is based on a second generation current conveyor CCII+ principle and its general scheme is shown in Figure 2. The whole monitor is connected between the VDD power supply and the *Virtual VDD* of the DUT. The CCII+ plays a main role in the monitor performance as it provides two important functions: it conveys the I_{DD} current to the output of the CCII+; and holds approximately the same voltage on both its input terminals. Thus, the deviation of the *Virtual VDD* from the VDD power supply is very small. Due to the fact that the DUT obviously draws high transient currents during switching actions, a bypass switch has been connected between the VDD and the *Virtual VDD* to bypass the monitor while the DUT is in the transient state.

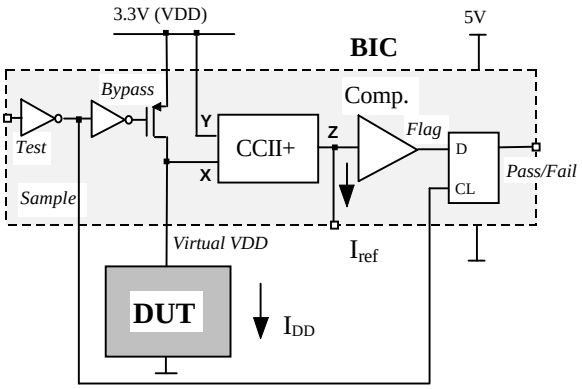

Figure 2 General scheme of the monitor

The output current of the current conveyor, which is equal to the I_{DD}, is then compared to the reference current I_{ref} by a current comparator and the signal *Flag* is produced as a result of the comparison. Since the comparison is performed continuously, control circuitry is added to sample the result of the comparison at the end of the measurement period. For the CCII+ as well as for the other circuits involved, a power supply of 5V is required.

2.1 The switch circuit

For high transient current peaks, the voltage drop across the CCII+ is too high. Therefore, a MOS switch is placed between the VDD supply and the *Virtual VDD* to bypass the monitor during transient currents. To achieve a voltage drop below 100mV (for transient peaks of 100mA), an equivalent switch resistance (ON state) of 1Ω should be used. Such a large switch may be split into several smaller cells, that allow a reduction of chip area if an application does not require to handle so high transient currents [12]. The switch used in the presented monitor consists of a PMOS transistor which has a size given by: L=0.7μm and W=15.72 mm for the 0.7μm CMOS technology.

No doubt that the switch is the crucial point of the monitor design because it is very important to

limit the charge injection through the parasitic capacitances of the huge bypass switch to the DUT circuit. Thus, a charge compensating PMOS transistor, connected in series with the main switch and actuated by a complementary signal, is inserted (Figure 3).

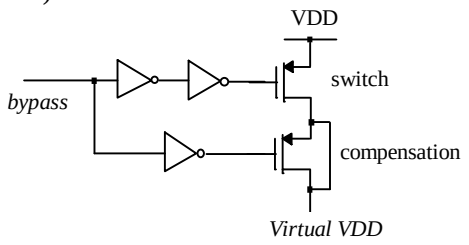

Figure 3 The compensated bypass switch

Simulations show that a good compensation requires the PMOS transistor with a size given by: L=0.7µm and W=1820µm for the whole switch.

2. 2 The control logic

In order to control the monitor circuit performance, additional logic has been used. Both, the *Bypass* and the *Sample* signals are generated from the single external input signal *Test*. The *Bypass* signal actuates the PMOS switch transistor and turns it from ON state to OFF one or vice versa. The *Sample* signal is used to clock a D Flip-Flop circuit at the end of the each clock period of the DUT, which samples the output of the current comparator.

3 Simulation results

The proposed monitor has been simulated using HSPICE and the monitor performance for nominal parameters, room temperature, testing frequency of 100kHz and a parasitic capacitance of the DUT C_{LOAD}= 50pF has been investigated in the range of supply currents from 50nA to 600A. Table 1 shows the accuracy of the I_{DDQ} current measurement for the condition mentioned above. It is worth underline that for I_{DDQ} currents in the range from 50nA to 10µA, the BIC monitor performs the current measurement with a very high accuracy of 10 nA.

Table 1

I_{DDQ} current	measured I_{DDQ} current	Accuracy
50nA	4 3nA	14%
100nA	92nA	8%
1µA	0.98 µA	2%
10µA	9.99 µA	0.1%
100µA	100.3 µA	0.3%
600µA	550 µA	8.3%

The proposed BIC monitor structure minimises the supply voltage degradation level during testing and the *Virtual VDD* is kept below 50mV in the whole range of I_{DDQ} currents.

Simulation results show that there is a strong relationship between maximal testing frequency and a value of the parasitic capacitance C_{load} . As for speed limitations, the presented quiescent monitor may be used for applications up to 1MHz testing frequency (for parasitic capacitance of the DUT of 200pF). If the required testing frequency is lower (5kHz), the monitor is able to drive a higher C_{load} (1µF). This offers the possibility to use the monitor also in off-chip current testing applications.

4 The layout implementation

Finally, the monitor circuit was implemented through Alcatel-Mietec 0.7µm CMOS technology. The layout was designed using Cameleon and Cadence design tools. The core of the chip layout is shown in Figure 6.

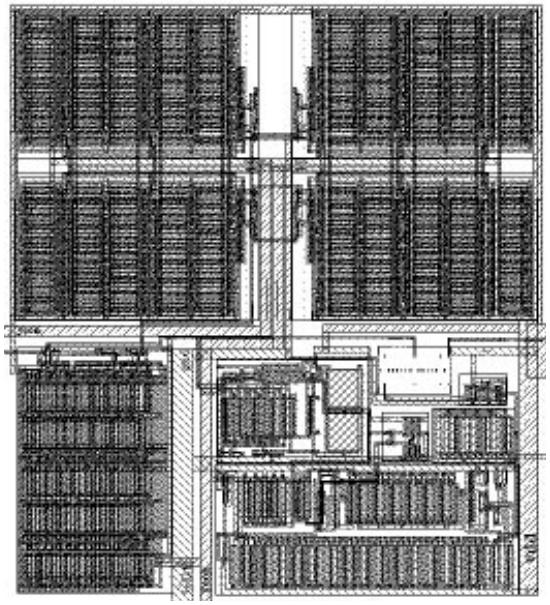

Figure 6 The core of the BIC monitor layout

The main chip area is occupied by the bypass switch that was splitinto 5 cells (5Ω each). For each 5Ω cell the layout has been structured into three parts: the main switch, the compensating switch and the driver block. The size of the whole 1Ω switch is 650µm x 205µm and each 5Ω section corresponds to 130µm x 205µm. Consequently, the total area of the quiescent BIC monitor is 0.22mm^2 and the bypass switch takes around 80% of the total area.

5 The evaluation of the chip

After fabrication, the evaluation of the prototype chips has been performed. The measurement of the circuit was realised on versatile PCB providing low parasitic capacitances and short connections. The BIC was placed in the socket DIL-18. Since, the use of a current source as the DUT is not possible because long wires would affect the measurement, the DUT was replaced by parallel R_L and C_L combination placed between pin X (*Virtual VDD*) and the GND.

The resolution of the monitor ΔI_N is given as a difference between pass and fail current levels. I_{FAIL} and I_{PASS} levels are measured values of I_{REF} current, when P/F output just became 'Low' or 'High', respectively. These levels are determined by noise that is the main limiting factor from the accuracy point of view. Table 2 indicates the resolution measurements for various C_{LOAD}. The supply voltage VDD was set to 5.0V and the voltage at the input Y to 3.3V according to the specifications.

Table 2

C_L⇨	10pF	100pF	1nF	10nF	100nF	1µF
0,100	0,6	28	190			
0,330	1	49	230	760		
1,00	3	75	400	1600	2400	
3,30	100	130	600	2300	5600	7400
10,0	230	420	900	3800	13000	19000
33,0	500	800	1300	7000	13000	24000
100	600	1100	1800	6000	16000	25000
330	1000	1000	1000	2000	2000	1000
1000	1000	1000	2000	2000	2000	2000
I_{DDQ}[µA]⇧	ΔI_N [nA]					

There is also a linearity error, in addition to the noise error ΔI_N, which represents deviations in I_{DDQ} measured by the monitor from the real I_{DDQ} value. Both the error items are included in the total relative error δI_{TOT} that expresses the maximal possible error of the current monitoring. Figures 4 shows the relative total current measurement error δI_{TOT} for various C_{LOAD}.

The evaluation results show the best resolution for low loading capacitances (C_{LOAD}< 1nF). The maximal resolution of the BIC monitor is 500pA at 5kHz test frequency, which is an excellent value.

As it has been already indicated by simulation results, the maximal testing speed strongly depends on C_{LOAD} and value of the current being measured. This relationship is graphically depicted in Figure 5. For high I_{DDQ} currents and low C_{LOAD} the maximal frequency of 2MHz is reached. This speed is very satisfactory with respect to the fact that I_{DDQ} testing is generally considered as a rather slow test method.

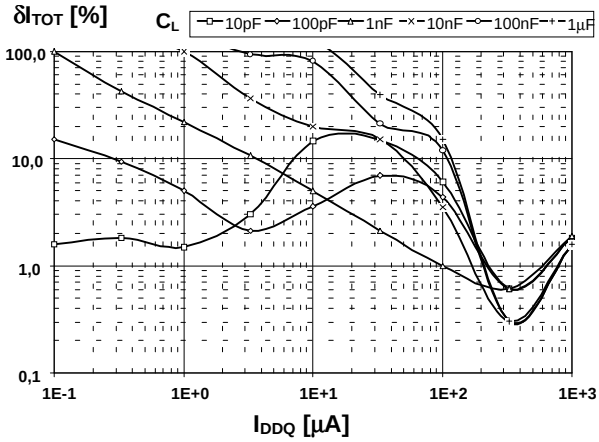

Figure 4 The total error given as $\delta I_{TOT}=\{ABS[(I_{PASS}+I_{FAIL})/2-I_{DDQ}]+\Delta I_N/2\}/I_{DDQ}$

Moreover, the evaluation shows the conveyor is capable to measure I_{DDQ} currents up to 500µA without any significant voltage (below 50mV) drop across it. For the quiescent currents up to 200µA, the deviation in the supply voltage is kept down below 1mV.

Additionally, deviations in the performance of the BIC monitor due to the supply voltage variations have been evaluated. Although, there was no significant influence found, it is worth noting that for higher values of the VDD, the BIC monitor could achieve much higher testing speed (especially for high I_{DDQ} and C_{LOAD}) but worse accuracy.

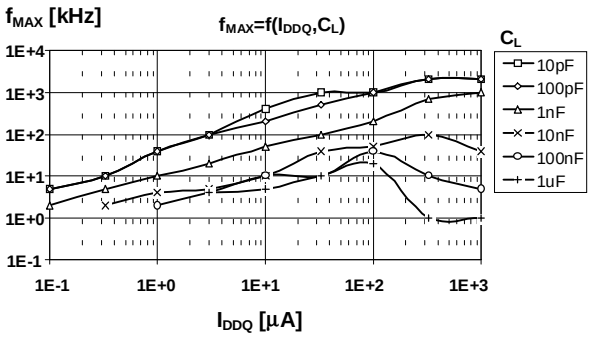

Figure 5 The maximal testing speed of the monitor

The only serious problem brought out during the chip evaluation is an undesired deviation in *Virtual VDD* due to charge injection through the bypass MOS switch's parasitic capacitances. Although, the voltage peaks, appeared during the switching actions of the bypass switch, are very narrow, the *Virtual VDD* reaches 4V (if C_{LOAD}=15pF) for this short time that may affect the performance of the DUT. However, the deviation is reduced with increasing value of C_{LOAD} and for C_{LOAD}=100pF the peaks are lowered to

250mV. This undesired effect could be limited by more precise compensation of the bypass switch that is considered to be realised in the future re-design.

6 Experimental usage of the monitor

Since the proposed BIC is able to perform the accurate measurement of supply current in a wide range of currents, an experimental implementation of the monitor in a new on-chip self test methodology for balanced current-mode analogue circuits has been consider [15]. To evaluate the feasibility of the BIC monitor for the new concurrent analogue self-test, a fault simulation was performed and a fully differential current conveyor was used as a DUT. Each of typical MOS transistor's terminal faults, shorts and opens, was individually injected into the DUT while the *Pass/Fail* output was monitored. Simulation results show that the new analogue self-test approach, that uses the current conveyor based BIC monitors, provides a fault coverage comparable to that achieved by previous methods based on a similar principle but with a much cheaper solution for no additional external equipment is needed.

7 Conclusion

A new quiescent current monitor circuit based on the current conveyor CCII+ has been reported. The I_{DDQ} current measurement approach mentioned in this paper is very sensitive and accurate in a range of I_{DDQ} currents from 50nA to 600µA. The proposed monitor was fabricated in Mietec 0.7µm CMOS technology and the evaluation of the prototype chips was done. The measurements show that the design of the monitor was successful and the results obtained overcame expectations in essential parameters. The best resolution of the monitor is 1nA at testing speed of 5kHz that is sufficient to detect any CMOS defect. The maximal testing speed of 2MHz can be achieved if the loading capacitance is low. In the whole operation range, the BIC monitor keeps the supply voltage degradation below 50mV. However, the bypass switch design should be improved in the future in order to reduce transfer of charge that results deviations in the power supply during transient states of the switch.

Although, the presented BIC monitor was originally supposed to be used for on-chip supply current monitoring, the results achieved indicate the possibility to use it also in off-chip applications accepting the proper accuracy and testing speed degradation.

Acknowledgment

This work has been supported by the EC in the frame of the COPERNICUS Project UBISTA (COP94:0391). Authors are very grateful to Michalis Sidiropulos for his help with providing the layout in Cadence design kit and to Bohumil Straka for providing the exhaustive evaluation of the chips.

References

[1] M.W. Levi, "CMOS is most testable", Proc. of ITC, pp.217-220, 1981

[2] Y.K. Malaiya and S.H.Y. Su, "A new fault model and testing technique for CMOS devices", Proc. of ITC, pp. 25-34, Philadelphia, PA, 1982

[3] J.M. Acken, "Testing for bridging faults (shorts) in CMOS devices", Proc. of Dig. Autom. Conf., pp. 717-718, San Francisco, CA, 1983

[4] C.F. Hawkins and J.M. Soden, "Electrical characteristics and testing considerations for gate oxide shorts in CMOS IC's", Proc. 1985 Test. Conf., pp. 544-555, Philadelphia, PA

[5] T.M. Storey and W. Maly, "CMOS bridging fault detection", Proc. of ITC, pp. 842-851, Washington, DC, 1990

[6] W. Mao, R.K. Gulati, D.K. Goel and M.D. Ciletti, "QUIETEST: A Quiescent Current Testing Methodology for Detecting Leakage Faults", Proc. of Int. Conf. on Computer Aided Design, pp. 280-283, 1990

[7] W. Maly and M. Patyra, "Built-in Current Testing", IEEE Journal of Solid State Circuits, pp. 425-428, Vol. 27, No. 3., March 1992

[8] W. Maly and M. Patyra, "Design of IC's Applying Built-In Current Testing", JETTA, 3, pp. 111-120, 1992

[9] J. Rius and J. Figueras, "Proportional BIC sensor for current testing", JETTA, Vol. 3, No. 4, pp. 387-396, 1992

[10] T.L. Shen, J.C Dali and J.C Lo, "A 2ns Detecting Time, 2µm CMOS Built-in Current Sensing Circuit", IEEE Journal of Solid State Circuits, Vol. 28, No. 1, pp. 72-77, 1993

[11] C. Hsue and C. Liu, "Built-in current sensor for Iddq in CMOS", Proc. of ITC, pp. 635-641, 1993

[12] A. Rubio, E. Janssens, H. Casier, J. Figueras, D. Mateo, P. De Pauw and J. Segura, "A built-in quiescent current monitor for CMOS VLSI circuits", Proc. of ED&TC 1995, pp. 581-585, Paris, France, March 1995

[13] A. Sedra and K. Smith, "A Second Generation Current Conveyor and its Applications", IEEE Trans. on Circuit Theory, Vol. CT-17, pp.132-134, 1970

[14] C. Tomazou, F.J. Lidgey and D.G. Haigh, "Analogue IC design: The current mode approach", pp. 93-127, P. Peregrinus Ltd., 1990

[15] M. Sidiropulos, V. Stopjakova and H. Manhaeve, "Implementation of a BIC Monitor in a New Analog Self-Test Structure", IEEE Inter. Workshop on I_{DDQ} Testing, Washington DC, USA, October 25, 1996, pp. 59-63.