Inductance Analysis of On-Chip Interconnects

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Abstract

It is generally believed that inductance analysis of on-chip interconnect becomes important when the clock frequency of circuits rise above GHz level. In this paper we show that this perception is not true. It becomes necessary to consider the inductive effects in all circuits implemented in deep submicron CMOS technologies. For 0.25 μm (lithography) technologies, where the supply voltage is expected to be in the range of 1.2-1.8 V, inductive effects are an important consideration regardless of system frequency. Furthermore, contrary to the popular belief, we show that inductive effects are important even for highly resistive lines.

1. Introduction

Analysis of inductive effects has always been important at chip packaging level and at the system level [1]. For digital circuits, the primary concern at chip packaging level is related to power supply distribution. Clocked circuits draw power in surges and results in supply and ground bounce. This is of particular concern in dynamic logic circuits where, multiple nodes may be precharged by a single clock simultaneously. Presence of uncompensated inductance on power lines may cause the power supply to ring with severe impact on noise and performance.

In analog circuits, designers are often concerned about transmission of noise from one part of the chip to other through the substrate because the substrate does not act as a true ground plane in presence of inductance[2]. The high frequency noise may find a lower resistance path through other nodes and devices rather than through substrate when the substrate has a high inductance connection to the ground. Thus, isolation of noise becomes a difficult issue.

At the card level, the rationale for studying inductive effect has been that in a RLC network, if R is low and ω is high, ωL becomes of significance in relation to R. The interconnect resistance in the card is deliberately kept low so that there is very little signal attenuation when signal travels over large distances across the card [3].

Traveling over distance of length l, signal amplitude on a resistive transmission line attenuates by $e^{-rl/2Z_0}$ where r, l, c are resistance, inductance and capacitance per unit length respectively and $Z_0 = \sqrt{l/c}$. Therefore it is not hard to understand the motivation for keeping r low.

Since on-chip interconnects look similar to interconnects on card, it is generally believed that the analysis technique should be the same. However, we point out that there are significant differences between on-chip signal interconnects and off-chip interconnects. The most important one has to do with impedance matching. For off-chip interconnects, the off-chip driver (receiver) resistance is adjusted to match the characteristic impedance Z_0 of the interconnects. For on-chip interconnects, the lines are not matched to loads. The on-chip interconnects drive a nonlinear capacitive load at the end which varies with signal and associated rise and fall times. It is impossible to engineer every interconnect receiver for matched impedance. Besides, any attempt to do that will increase the chip area very significantly.

The next important difference is the fact that on-chip interconnects are highly resistive. On-chip interconnects have to shrink in tandem with devices to realize increased density on a chip. Thus the interconnects become more resistive in newer generations of technology. Since most interconnect lengths are small, signal attenuation has not been a concern. It was believed that this trend will counter the need for inductance analysis of on-chip interconnects [4]. However, in section 3 of this paper we dispel this notion by showing that inductive coupling can introduce significant effects on highly resistive lines.

What are the inductive effects of relevance? When an interconnect response is over damped, it contributes to delay [4, 5]. If it is under damped it may contribute to noise. However, noise analysis is extremely complicated because of the fact that the only noise that matters is what is seen by the receiver. Due to mismatched impedances along on-chip interconnects (compounded by presence of vias) there are multiple reflections and signal waves traveling backward and forward. The coupled sources of noise inject further noise signals at many intervals. The effect of all these noise signals may peak at a point different from the receiver location and therefore may not matter for the chip performance. However, such analysis even for a single net is impossible to achieve because it requires an exact extraction of capacitances and inductances (recognized to be a difficult task), needs boolean relationships between various nets, needs precise arrival time of these signals (which requires the same analysis to be performed on all nets that contribute to the signal of interest, recursively backwards with possible boolean combinations).

However, conservative approximation is not hard to arrive. This is based on the premise that all coupled nets are hostile and all coupled noise voltages collide at the receiver in the worst possible way.

In this paper, we go through a very simple calculation to show that inductance matters for on-chip interconnects. With conservative approximations, they can be analyzed and taken into design considerations.

2. Total Inductance of On-Chip Interconnect is Variant With Time

In this section we show that the total inductance of on-chip interconnects vary with time. The total inductance on a conductor is composed of self and mutual inductances. Analysis of inductive effects

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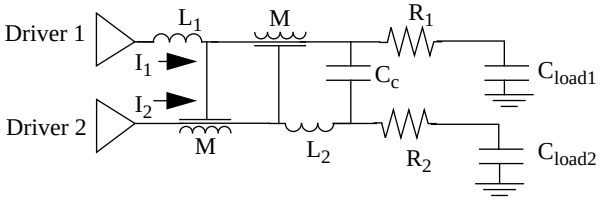
also need to take the drivers of inductively coupled nets into consideration. For example, let us consider the two nets in the system as shown in the figure below. For the purpose of illustration, the distributed RLC model has been lumped by single elements, where R_1, L_1 are lumped line resistance of line 1 and M, C_c are mutual inductance and coupling capacitance respectively. For greater accuracy one could use a higher order lumped Π model, however the simplified model is enough to drive the main point of this section. The total inductance seen from driver 1 is $L = L_1 + M\dot{I}_2/\dot{I}_1$. Since $\dot{I}_1$ and $\dot{I}_2$ are time varying functions, it is readily seen that the total inductance of the interconnect also varies with time.

This is totally distinct from off-chip interconnects where the slew rate of all drivers are adjusted to be same. Thus, for off-chip interconnects total inductance is often assumed to be linear sum of self and all mutual inductances ($L_1 + M$).



3. Highly Resistive Lines May Have Significant Inductive Effects

Suppose R_1 is very high. This implies that $\dot{I}_1$ is very low. Thus, for driver 2, effect of M may be very little. If R_2 is sufficiently low then $\dot{I}_2$ could be high, resulting in a significant inductive effect on line 1. Therefore it is readily seen that just because a line is highly resistive does not mean that it is immune to inductive effects.

Conclusions in Sections 2 and 3 would be of minor significance if:

1. $L\dot{I}$ is not of significance relative to V_{dd} and
2. M is not of significance relative to L

So we have to show that $L\dot{I}$ is of significance relative to V_{dd} and M is of significance relative to L. This is what we do next.

4. Inductance Calculation

In order to show that on-chip inductive effects are of significance we have to know the values of L, M and $\dot{I}$. We assume that on-chip metal lines have rectangular cross section and at 0.25 μm lithography, the lines are $0.4\mu m$ wide and $0.4\mu m$ apart and $0.6\mu m$ thick. The intra-layer dielectric thickness is assumed to be 0.8 μm. These assumptions will be used to calculate some representative values, other than that they are not of much significance. As it turns out later in this section, that the inductance values are not very sensitive to these values. Thus getting the order of these numbers is important, but the actual numbers are not that important. The important components are self inductance and mutual inductance.

4.1. Calculation of Self Inductance

Let, the length of the line be l, and the width and thickness be W and T respectively. Defining the normalized width and thickness as $w = \frac{W}{l}$ and $t = \frac{T}{l}$ and some extra parameters $r = \sqrt{w^2 + t^2}$, $\alpha_w = \sqrt{w^2 + 1}$, $\alpha_t = \sqrt{t^2 + 1}$ and $\alpha_r = \sqrt{w^2 + t^2 + 1}$, the self inductance can be written as [6]:

$$
\begin{aligned}
\frac{L}{l} = \frac{2\mu}{\pi}\Bigg| & \frac{1}{4}\left[\frac{1}{w}S\left(\frac{w}{\alpha_t}\right) + \frac{1}{t}S\left(\frac{t}{\alpha_w}\right) + S\left(\frac{1}{r}\right)\right] \\
& + \frac{1}{24}\left[\frac{t^2}{w}S\left(\frac{w}{t\alpha_t\left(r+\alpha_r\right)}\right) + \frac{w^2}{t}S\left(\frac{t}{w\alpha_w\left(r+\alpha_r\right)}\right)\right] \\
& + \frac{1}{24}\left[\frac{t^2}{w^2}S\left(\frac{w^2}{tr\left(\alpha_t+\alpha_r\right)}\right) + \frac{w^2}{t^2}S\left(\frac{t^2}{wr\left(\alpha_w+\alpha_r\right)}\right)\right] \\
& + \frac{1}{24}\left[\frac{1}{wt^2}S\left(\frac{wt^2}{\alpha_t\left(\alpha_w+\alpha_r\right)}\right) + \frac{1}{w^2t}S\left(\frac{w^2t}{\alpha_w\left(\alpha_t+\alpha_r\right)}\right)\right] \\
& - \frac{1}{6}\left[\frac{1}{wt}T\left(\frac{wt}{\alpha_r}\right) + \frac{t}{w}T\left(\frac{w}{t\alpha_r}\right) + \frac{w}{t}T\left(\frac{t}{w\alpha_r}\right)\right] \\
& - \frac{1}{60}\left[\frac{\left(\alpha_r + r + t + \alpha_t\right)t^2}{\left(\alpha_r + r\right)(r+t)\left(t+\alpha_t\right)\left(\alpha_t+\alpha_r\right)}\right] \\
& - \frac{1}{60}\left[\frac{\left(\alpha_r + r + w + \alpha_w\right)w^2}{\left(\alpha_r + r\right)(r+w)\left(w+\alpha_w\right)\left(\alpha_w+\alpha_r\right)}\right] \\
& - \frac{1}{60}\left[\frac{\left(\alpha_r + \alpha_w + \alpha_t + 1\right)w^2}{\left(\alpha_r + \alpha_w\right)\left(\alpha_w+1\right)\left(\alpha_t+1\right)\left(\alpha_t+\alpha_r\right)}\right] \\
& - \frac{1}{20}\left[\frac{1}{r+\alpha_r} + \frac{1}{\alpha_w+\alpha_r} + \frac{1}{\alpha_t+\alpha_r}\right]\Bigg| \qquad (1)
\end{aligned}
$$

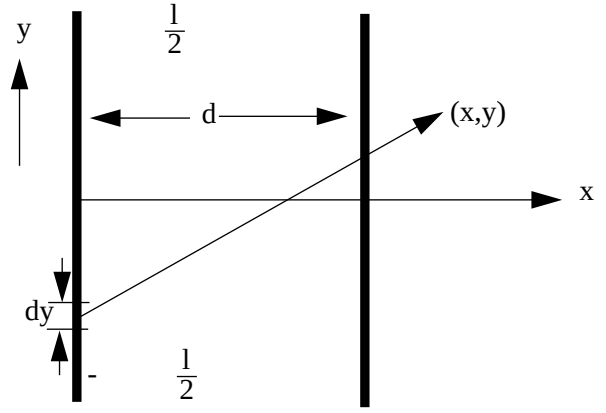
where, $S(x) = \ln\left(x + \sqrt{1+x^2}\right)$ and $T(x) = \text{atan}(x)$.

At filament approximation (T,W << l), the expression can be simplified by the following formula [7]:

$$\frac{L}{l} = \frac{2\mu}{\pi}\left[\ln\left(\frac{2l}{0.2235\,(W+T)}\right) - 1\right] \qquad (2)$$

4.2. Calculation of Mutual Inductance

Mutual inductance between two structures depend mainly on the relative geometrical position and the length of the wires rather than the shapes. The mutual inductance between two filaments was calculated in [8], based on Biot-Savart law [3]. Calculation involves flux linkage by one conductor due to the other. M was derived as:



$$\frac{M}{l} = \frac{\mu}{2\pi}\left[-\sqrt{1+\left(\frac{d}{l}\right)^2} + \frac{d}{l} + \ln\left(\frac{l}{d} + \sqrt{1+\left(\frac{l}{d}\right)^2}\right)\right] \qquad (3)$$

For $d \ll l$, the expression simplifies to

$$\frac{M}{l} = \frac{\mu}{2\pi}\left[\ln\left(\frac{2l}{d}\right) - 1\right] \qquad (4)$$

From these expressions, one can see that L and M are close for the typical wire dimensions in 0.25 μm technology. Unfortunately, one cannot generalize from the result of two isolated wires, because presence of other nearby structures modify the current in conductors and shape the field lines differently. However, the general pattern of relationship between L and M holds which was the basis of conclusions in Sections 2 and 3.

4.3. Self and Mutual Inductances in Presence of Other Conductors

We have to make certain assumptions in order to use an extraction tool to find L and M. The assumptions we make are that (1) the wiring planes above and below are running orthogonal, which is usually the case; (2) the loading in planes above and below is 50%, which may be somewhat true; (3) the planes above and below are ground planes (which is a standard assumption made in 2D capacitance and inductance extraction), an assumption made on the basis of the fact that some of the lines are actually ground lines, some others are friendly (switching in the same direction) and some others are hostile (switching in the opposite direction) with a net contribution approximating a ground. Discussions in Section 2, should be enough of a caution against making such gross assumptions, however such assumptions are necessary for extraction tool to run. Pattern dependent extraction is impractical with today's computational resources, but may become practical in some future date. Currently available extraction tools are pattern independent. This exposes a limitation of our current extraction technology. Using a commercial tool, L and M are calculated to be 5.3 nH/cm and 3.3 nH/cm respectively for the assumed geometry in the beginning of Section 4.

5. On-Chip Inductive Effect Calculation

In the previous section, we have established some reference values of L and M. Next we show, that $L\dot{I}$ is significant when compared with V_{dd}. In order to do that let us assume that an inverter is driving a RLC line.

The saturation current I_{ds}, that flows through a transistor in the inverter is governed by the following equation:

$I_{ds} = \beta (V_{dd} - V_t)^{\alpha}$ [9],

$\beta = \frac{\mu\varepsilon}{t_{ox}}\frac{W}{L}$,

μ is mobility of electrons/holes in the channel,

ε is permittivity of $SiO_2 = 3.9 \times 8.854 \times 10^{-12}$ F/m,

t_{ox} is oxide thickness,

W is the width of the transistor,

L is the effective channel length of the transistor,

V_t is the threshold voltage

The rise and fall time associated with the inverter output can be approximated as

$\tau = \Upsilon\frac{C_l V_{dd}}{I_{ds}}$,

where Υ is a constant somewhere between 3 and 4 [10] and

C_l is the load capacitance.

The current I_{ds} gets switched in time τ, so

$$\dot{I}_{ds} = \frac{I_{ds}}{\tau} = \frac{I_{ds}^2}{\Upsilon C_l V_{dd}} = \frac{\beta^2 (V_{dd} - V_t)^{2\alpha}}{\Upsilon C_l V_{dd}}$$

or,

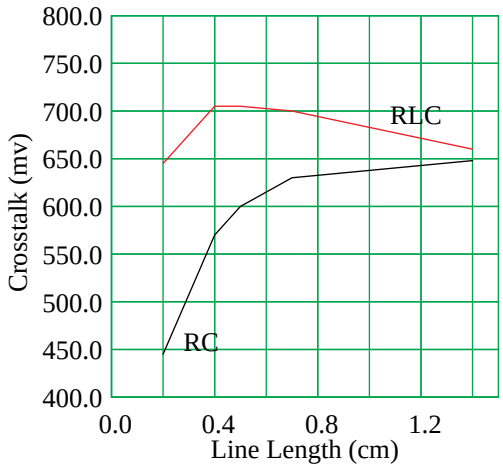
$$\frac{L\dot{I}}{V_{dd}} = L\frac{\beta^2 (V_{dd} - V_t)^{2\alpha}}{\Upsilon C_l V_{dd}^2}$$

For interconnects with length of the order of mm, $C_{interconnect} \gg C_{receiver}$ and hence, $C_l \approx C_{interconnect}$. Therefore,

$$\frac{L\dot{I}}{V_{dd}} = Z_0^2\left(\frac{\beta^2 (V_{dd} - V_t)^{2\alpha}}{\Upsilon V_{dd}^2}\right) \qquad (5)$$

The equation above indicates that if effect due to mutual inductance can be ignored, *the inductive noise does not depend on interconnect length. In fact, due to presence of resistance the inductive noise effect will be smaller for longer interconnects.* This conclusion is also supported by simulation on extracted models. There is a greater dependence on driver size (β factor). The simulation scenario is described below.

For the purpose of simulation a RLC model was extracted for metal lines in the second layer with a single switching line inducing noise in an adjacent line. The tracks in upper and lower layers run orthogonal to the one under consideration. All tracks in layers above and below are assumed to be occupied with lines connected to ground. The switching line is driven by an inverter with a step input whose NFET is 100 µm wide and PFET is 200 µm wide. The devices have a nominal effective channel length of 0.25 µm and the power supply voltage is 2.5 V. Switching noise is measured at the far end of the coupled line. The near end is connected to ground. The results of the experiment is shown next. Please note that in this simulation study, the driver strength will match the load only at a specific interconnect length. For all other cases the drive is either excessive or deficient.



Example: Let the capacitance per unit length and the inductance per unit length be 2 pF/cm and 5 nH/cm respectively. This implies Z_0 = 50 Ω. Let the driver width = 50 µm, I_{ds} per micron of gate width = 0.5mA, $V_{dd} = 1.8V$ and $\Upsilon = 4$.
Then, net $I_{ds} = 50 \times 0.5 = 25$ mA

and $$\frac{L\dot{I}}{V_{dd}} = \frac{5 \times 10^{-9}}{2 \times 10^{-12}} \frac{(25 \times 10^{-3})^2}{4 \times 1.8^2} = 0.12 \quad .$$

This shows that inductive effect can be as much as 12% on a net. This effect goes up more with bigger driver size. The driver size goes up with driven interconnect length. However for a given driver size the net effect is some what independent of net length.

6. Conclusions

We showed that for a matched load, inductive effects are significant at 1.8V technology (12%). For matched load at 2.5V inductive effects were not as pronounced (around 6%) and at 3.3V they were even lower. With this paper we tie inductive effects to supply voltage and technology scaling rather than frequency as has been the case in the past. We further showed that inductive effects can appear on highly resistive lines as well. These issues will be very important for analyzing on-chip interconnections in 0.25 µm CMOS designs and beyond.

7. References

[1] B. J. Rubin, ‘‘An electromagnetic approach for modeling high-performance computer packages,’’ *IBM J. of Res. and Develop.*, vol. 34, pp. 585-600, July 1990.

[2] D. K. Su, M. J. Loinaz, S. Masui, B. A. Wooley, ‘‘Experimental results and modeling techniques for substrate noise in mixed signal integrated circuits,’’ *IEEE J. Solid-State Circuits*, vol. 28, pp. 420-430, April 1993.

[3] S. Ramo, J. R. Whinnery, T. Van Duzer, *Fields and Waves in Communication Electronics*, John Wiley & Sons, New York.

[4] J. R. Brews, ‘‘Overshoot controlled RLC interconnections,’’ *IEEE Trans. Electron Devices*, vol. 38, pp. 76-87, Jan 1991.

[5] J. L. Wyatt, Jr., ‘‘The practical engineer’s non-nonsense guide to on-chip signal delay calculations,’’ *VLSI Memo. No. 87-381*, MIT, May 1987.

[6] A. E. Ruehli, ‘‘Inductance calculation in a complex integrated circuit environment,’’ *IBM J. of Res. and Develop.*, vol. 16, pp. 470-481, Sept. 1972.

[7] F. W. Grover, *Inductance Calculations: Working Formulas and Tables*, Van Nostrand, New York, 1962.

[8] A. J. Rainal, ‘‘Computing inductive noise of chip packages,’’ *AT&T Bell Lab. Tech. J.*, vol 63, pp. 177-195, January 1984.

[9] T. Sakurai and A.R. Newton, ‘‘Alpha power law MOSFET model and its applications to CMOS inverter delay and other formulas,’’ *IEEE J. Solid-State Circuits*, vol. 25, pp. 584-594, April 1990.

[10] N. H. E. Weste and K. Eshraghian, *Principals of VLSI design: A Systems Perspective*, Addison Wesley, New York, 1993.