Automatic Transfer of Parametric FEM Models into CAD-Layout Formats for Top-Down Design of Microsystems

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Abstract

A tool for the transfer of solid models used for FEM simulations into different layout formats used by CAD environments is presented. All necessary layers for the fabrication of microcomponents and -systems in a given extended commercial CMOS process are generated automatically by this tool. Starting with an acceleration sensor the use of this translator for an application in the top-down design of microsystems with parametric components is described.

1 Introduction

The design of microelectromechanical systems today is characterized by the lack of powerful design environments which can support the system designer as well as the component designer. Such tools are known in the microelectronic world for a long time and therefore, they are a good starting point for the development of new tools or interfaces with features which are important for the microsystem design. For microsystems which have very specific functions or which are difficult to fabricate - perhaps only on special non-standardized fabrication lines - it will always be difficult to create support tools which assist the designer from the beginning to the end of the design process. However, regarding microsystems which are based on existing and fixed fabrication lines - whether it's a special micromechanical process, a bipolar process [1] or a CMOS-compatible process [2] - such tools are suggestive and possible. In the recent years, a lot of approaches have been published which assist the designer on the system level [3,4]. In contrast, design tools for MicroElectroMechanicalSystems on a lower level are quite rare.

In this paper we present an approach for the low-level design support, i.e the layout level. A translator which generates all layers necessary for the fabrication of microcomponents in a commercial CMOS process is introduced. These layers are derived from a solid model used in a FEM simulator. This translator can easily be adapted to other reproducible processes that are characterized by design rules.

2 Using a CMOS process for MEMS design

In order to achieve a good performance of microsystems and because of the good knowledge of microelectronic processes a lot of microsystems are fabricated in a CMOS-compatible process. This gives the opportunity to put e.g. micromechanical components and the belonging signal processing unit together easily. Even some designs using a extended commercial (Bi)CMOS process with one or more additional micromachining steps are made so far [2]. Additionally the application of existing microelectronic processes gives the opportunity to fabricate devices cheaply and in high volumes.

Since the beginning of 1996, CMP Grenoble provides the opportunity to take part in a multi-chip-project for MEMS. A commercial 1.0µm CMOS process (ES2) is followed by an additional anisotropic etch step which releases suspended structures. Complete designs can be realized, which integrate microelectronics and e.g. micromechanics monolithically. The design rules for micromachined structures in this process can be received from CMP. CMP also provides some utilities which assist the designer in the development of own microsystems [5]. Especially for the inclusion of predefined parametrized components these tools are very helpful. But if own totally new designs are to be included, all design steps have to be done by hand. Like in a full custom design in microelectronics each layer has to be drawn separately. In the case of the above mentioned CMOS process the suspended structures consist of at least four different layers, which are also used in this CMOS process for microelectronic components. These layers are not identical

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(from the geometric point of view) but have an certain overlap over each other. The minimal dimensions for this overlap are given by the process dependent design rules. If the geometry of the design gets more complicated, the drawing of the corresponding layers gets more and more difficult and susceptible to faults.

As in most cases FEM simulations are done in the first design phase of microsystems, the corresponding solid models can be used for an automatic transfer into a mask layout for the following fabrication process. Moreover, the modeling of solid models in a FEM simulator like ANSYS is easier and more comfortable than drawing layout masks. The presented automatic conversion allows an easy and fast mask generation without errors.

3 Automatic mask generation out of a FEM model

The FEM simulator used as starting point for our tool is ANSYS[1]. ANSYS provides the opportunity to extract all relevant geometric parameters which are necessary to create the mask layout. The generated output can either be a CIF or an EDIF file, which can be read by most of the layout editors, in our case Cadence DFW II[2].

In a first step, the overall geometry of the FEM model is extracted and saved in separate files with all keypoints, lines and areas belonging to it. This can be done interactively using ANSYS. In a next step these data are read into the converter. After all geometric operations and conversions as described in the following are done, the layout information is stored in a new CIF or EDIF file just using polygon declarations (no path nor box declaration is necessary).

3.1 Possible geometric operations

In a FEM simulation the body of a structure itself is modelled and used for further calculations. In the layout of this structure it is vice versa. The body itself is not considered but the free area surrounding it. This is because the drawn layers mark the area where the etchant attacks the monocrystalline silicon and starts the micromachining process step. The area which is not covered by the layer will rest as suspended structure.

For that reason the geometry given by the FEM model has to be inverted. This can be seen in figures 1,2 which show on the one hand an ANSYS model of the half of a membrane with a suspension arm and the boundary of the etch hole, and on the other hand the automatically generated corresponding layout. The hatched areas show the parts which are removed during etching, so the white area rests as suspended structure.

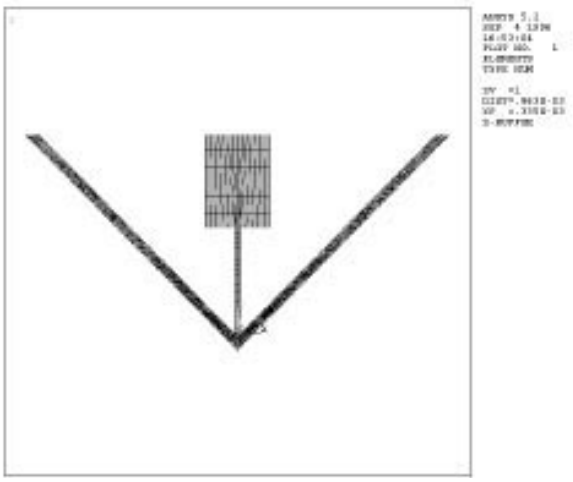

Figure 1 : ANSYS model of a suspended membrane

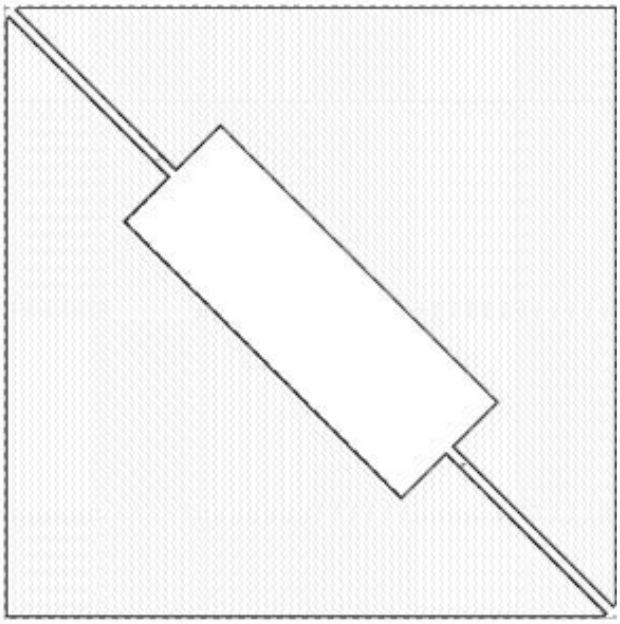

Figure 2: Cadence layout of a suspended membrane

Furthermore, it can be seen in figure 1 that only one half of the total membrane geometry is modelled for the FEM simulation. This is done because of symmetry reasons and helps saving time in simulations. As this procedure is often used in finite element analysis, a mirroring option is included in our translator. Mirroring at a single point as well as at a line is possible. In a final step the model also can be turned in the drawing plane. This is necessary in most cases, because the relevant structures in a FEM

[1] ANSYS is a registered trademark of Swanson Analysis Systems, Inc.

[2] Design Framework II is a trademark of Cadence Design Systems, Inc.

simulation are aligned along the principal axis, that means a horizontal/vertical alignment. In contrast to this, the real structures - meaning the masks - are placed diagonally, because this is - in the here used process - the direction of the <100> planes. These planes are etched much faster than the horizontal/vertical oriented <111> planes and therefore preferred for forming the suspended structures.

After the generation of the principal mask, the other three layers which are necessary for designing suspended structures are zoomed out by a certain offset. This offset is given, as mentioned before, through the guidelines and design rules for the used process .The final shape of all masks can be seen in figure 3.

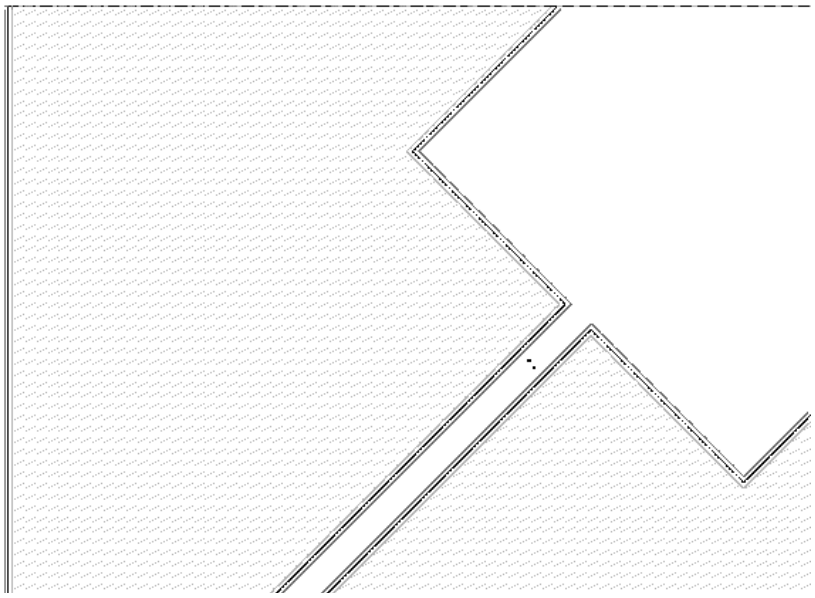

Figure 3: Section of the layout showing the mask shape

In order to keep the universally valid character of the translator and not to limit the use only for special processes, all possible geometries are allowed. Convex polygons as well as concave ones, circles and areas with wholes are valid even if not all geometric bodies are needed as in the case of the herein used 1.0µm CMOS process.

In a last step additional layers which are optional for the design, such as metal layers for connection or for increasing the weight, polysilicon layers or vias, can directly be generated by keypoints representing the edges of the desired shape. Existing keypoints referring to other layers or new ones represented by new coordinates are a valid input.

For all generated layers the spacing of the underlying grid can be chosen in dependence of the properties of the process in order to get a correct snapping of the edges of each area. Additionally, one can choose a separate scaling factor (DatabaseUnit per UserUnit) in order to get a correct read-in into the used layout editor.

The third dimension of microsystems normally is not represented in a mask layout, but is inherently given by the mask shape and sequence and by the process parameters. Therefore, the third dimension, even if given in a FEM simulation, can be neglected. For a lot of applications in microsystem technology a FE representation with only 2-D elements like shells is sufficient. In that case the translation into a layout can be done directly. If a 3-D-representation in ANSYS is used, what is obviously necessary sometimes as the real world is three-dimensional, the dominating keypoints in the model have to be selected in ANSYS before the translation.

The presented converter is written in C++ code and implemented on UNIX-Workstations. For an easy use it is equipped with an Motif based graphical user interface. All options mentioned above can directly be accessed through this GUI.

4 Top-down design for parametric MEMS demonstrated with an acceleration sensor

The above presented tool can be used in two ways. On the one hand, as mentioned before, it just serves as a support tool for an easy mask generation.

On the other hand, what might be more important, already given designs can be adjusted in geometry for changing properties. For example the membrane given in

figure 2, which is part of an acceleration sensor [6], can be adapted to predefined requirements. When changing the width or the length of the suspension arms or the membrane itself the behaviour of the acceleration sensor (e.g. sensitivity, maximum acceleration) changes as well. To meet given requirements all relevant analysis and changes in geometry can be made with ANSYS. Afterwards, the new design will be exported into a layout format for further use in a microelectronic CAD environment. As the acceleration sensor exists as parametric FEM model, the above mentioned adjustment can be achieved easily. Together with the behavioural model of this sensor in HDL-A[3] [7] a complete description of the microcomponent is available. Complete simulations of complex systems on behavioural level, e.g. with ELDO[3] are possible this way.

Figure 4 shows the concept of a top-down design flow with this tool: a parametric FEM model of a microcomponent - here the acceleration sensor - is the base for the generation of a set of layout-masks and HDL-A models as well. These models and mask sets are generated by our FEM2CIF/EDIF translator and the FEM2HDLA translator [3] respectively and can be stored in a database.

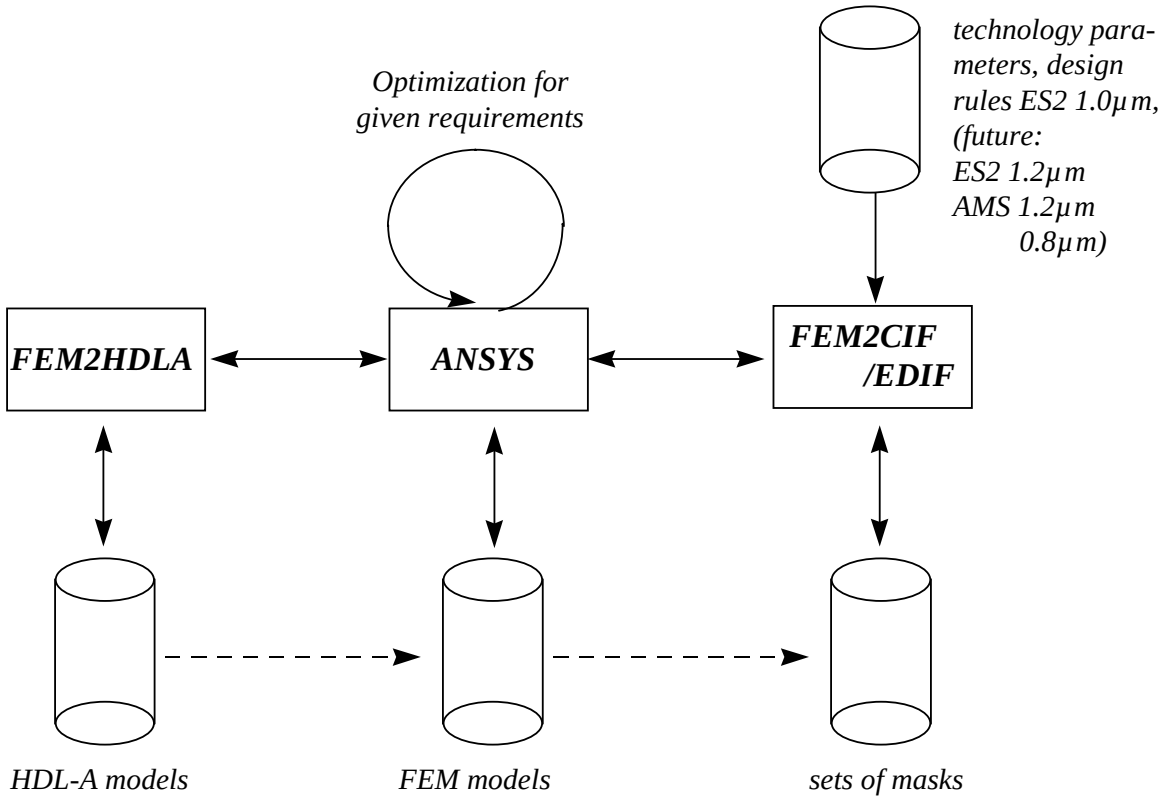

Figure 3: top-down design flow for microcomponents

As far as only few sets are available, always FEM simulations will deliver the desired design, and a translation in HDL-A[3] and mask sets will start from this point. But if more and more models exist, a direct connection from the behavioural description down to the layout will be established. Starting with an HDL-A model which nearly fulfils certain requirements, the corresponding FEM model and the layout masks can be used directly or adapted slightly if necessary.

The presented converter has been conceived for, but is not limited to the use of the above mentioned 1.0µm CMOS process (ES2). The operation of mask generation can easily be adapted to other processes with other parameters, e.g. other CMOS processes with other minimum dimensions or other design rules. Also the use in pure micromechanical processes is possible.

[3] HDL-A and ELDO are trademarksof ANACAD EES Ltd.

5 Conclusion and Outlook

In this paper we have presented a translation tool which produces layout masks in EDIF or CIF format out of a FEM model. This translator permits an easy and fast transfer of designs in a format ready for fabrication. Moreover, this tool gives the opportunity to extract correct layout masks from a parametric FEM description in order to adapt devices to personal requirements.

Up to now, our tool generates new sets of masks each time. So future work will be done on the option to change given CIF or EDIF files. This option will allow to change only parts of a complex design without distorting or erasing the non-affected part (e.g. included microelectronics, signal processing). Moreover, a transfer the other way round is planned, meaning the possibility to create a solid model for FEM simulations out of a mask description. In this version the design rules concerning the minimum overlap of the layers are given as input in the graphical user interface. For future versions the technology file of the process will be read automatically and the parameters for the overlap will be adjusted in dependence of the used process.

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