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## ED&TC '97

European Design & Test Conference

Paris, France
March 17-20, 1997



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# The European Design & Test Conference 1997


FROM ASICs TO SYSTEMS

# Proceedings

Paris, France
March 17–20, 1997

Sponsored by
European Design and Automation Association
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Proceedings

# European Design & Test Conference

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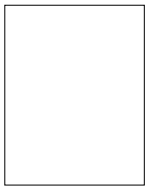

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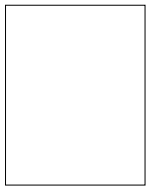

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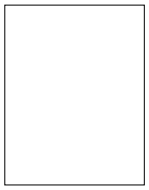

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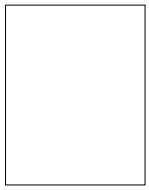

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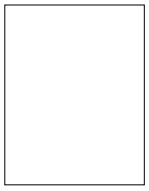

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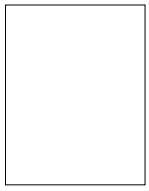

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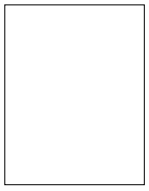

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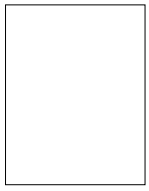

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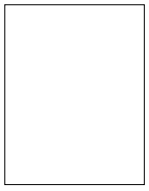

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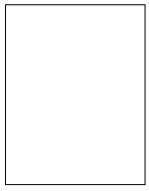

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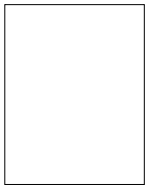

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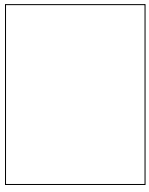

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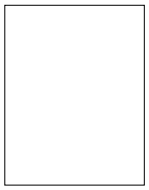

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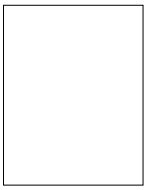

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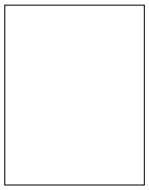

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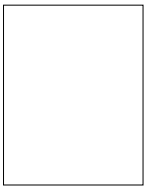

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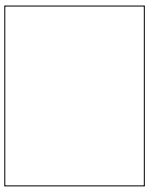

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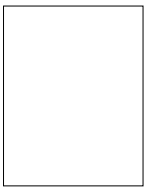

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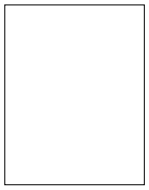

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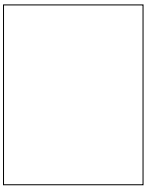

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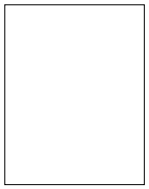

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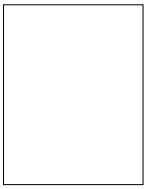

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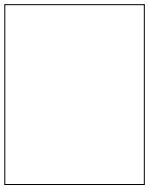

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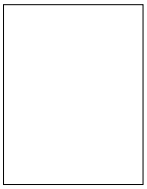

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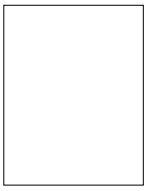

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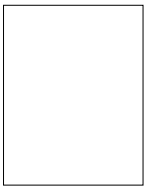

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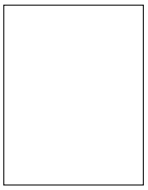

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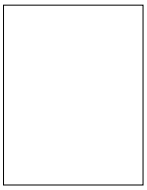

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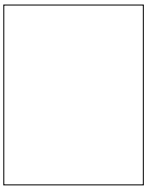

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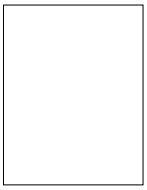

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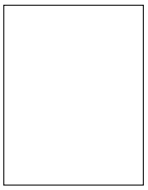

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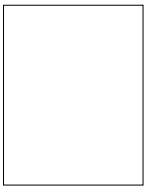

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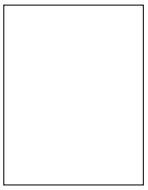

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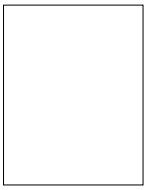

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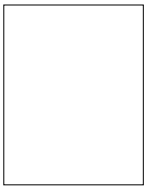

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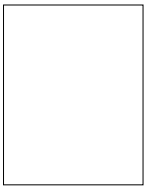

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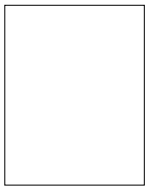

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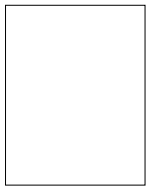

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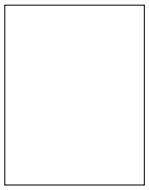

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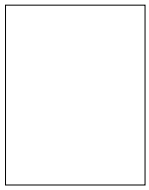

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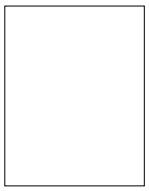

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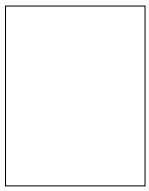

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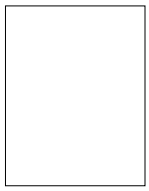

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Hidetoshi Onodera, Kyoto University, Japan
Ralph Otten, Delft University of Technology, The Netherlands
Jeannie Panner, IBM Corp., USA
Lalit Patnaik, Indian Institute of Science, India
A. Peyre-Lavigne, Motorola R&D, France
Juha Pikkarainen, Nokia Mobile Phones, Finland
Serge Pravossoudovitch, LIRMM, France
Paolo Prinetto, Politecnico di Torino, Italy
Janusz Rajski, Mentor Graphics Corp., USA
Andrew Richardson, Lancaster University, UK
Manoj Sachdev, Philips Research Laboratories, The Netherlands
Ryo Sano, Advantest Corp., Japan
Majid Sarrafzadeh, Northwestern University, USA
Gabrièle Saucier, INPG/CSI, France
Rolf Schlagenhaft, Technical University of Munich, Germany
Bernd Schuermann, University of Kaiserslautern, Germany
Peter Schwarz, FhG IIS/EAS Dresden, Germany
Donatella Sciuto, Politecnico di Milano, Italy
Carl Sechen, University of Washington, Seattle, USA
Rene Segers, Philips Semiconductors, The Netherlands
Michal Servit, Czech Technical University, Czech Republic
J.P. Singleton, ICL, UK
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M. Strik, Philips Research Laboratories, The Netherlands
Vladimir Szekely, Technical University of Budapest, Hungary
Yago Torroja, Univ. Politecnica de Madrid (UPM), Spain
Raimund Ubar, Tallinn Technical University, Estonia
Pieter van der Wolf, Philips Research Laboratories, The Netherlands
Jef van Meerbergen, Philips Research Laboratories, The Netherlands
H.T. Vierhaus, Technical University of Cottbus, Germany
Frank Walzer, Texas Instruments, Germany
Wayne Wolf, Princeton University, USA
Hans Joachim Wunderlich, University of Stuttgart, Germany
Hiroto Yasuura, Kyushu University, Japan
Yervant Zorian, LogicVision, USA

*Keynote Address*

# Intrinsic (but not insurmountable) Barriers to Gigascale Integration (GSI)

James D. Meindl
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Opportunities for GSI are governed by a hierarchy of limits whose five levels can be codified as: fundamental, material, device, circuit and system. This constructive methodology is extended here by elucidating the impact on GSI of random dopant atom placement in the channel region of a MOSFET and random interconnect placement in binary logic networks. Random microscopic fluctuations in the number and location of dopant atoms in the channel depletion region of a MOSFET induce stochastic variations in device parameters such as threshold voltage, subthreshold swing and drain current. The standard deviations of these parameter distributions increase as device dimensions are scaled down. These increases in combination with concurrent upward scaling of the number of MOSFETs per chip cause a rapid escalation of the maximum deviations of MOSFET parameter values for the ensemble of devices within a given die. At some value of maximum deviation of threshold voltage, for example, faulty operation of logic circuits ensues. The effective channel doping concentration F(na), the threshold voltage F(Vts), the subthreshold swing F(S), and the drain current F(Idsat) distribution density functions for a MOSFET with a nominally uniform channel doping profile have been determined. Calculations of the standard and maximum deviations of threshold voltage, Vt , across the technology generations projected by the US National Technology Roadmap for Semiconductors (NTRS) indicate alarmingly large 45-89% maximum deviations of threshold voltage for the NTRS 2010 or 0.07mm generation of chips. For more than three decades, Rent's rule has proven to be a useful empirical relationship between the number of logic gates in a block, Ng , and the number of signal input/output interconnects, Ni/o , of the block. The form of the relationship is Ni/o =3D K(Ng)p, where K and p are= empirical constants. Rent's rule has been applied recursively to a square array of logic gates for the purpose of deriving the complete stochastic wire length distribution of the array including local, semi-global and global interconnects. For an array of 34.4 million gates assumed to be implemented with 0.l micron or 2007 generation technology in a die area of 1100 mm2, this distribution density function is typically described by values of K in the range of 4 and p in the range of 0.6. The chip includes approximately 107 wires less than three gate pitches in length and a single wire 6,700 gate pitches in length. About 93% of the wires are less than 25 gate pitches in length and consume only 23% of the total interconnect length on the chip. Interconnects longer than 220 gate pitches constitute 50% of the wiring demand, but only 1.1% of the number of interconnects, which underscores the importance of working with a complete wiring distribution including all global wiring in preparing a priori estimates of chip wiring demand.

*Keynote Address*

# Systems on a Chip: The Electronics Industry at a Crossroads

Dr. Aart J. de Geus
President and CEO
Synopsys, Inc.

The electronics industry is moving rapidly toward the ability to integrate a combination of electronic systems onto a single chip. This paradigm shift, from placing chips on boards to combining electronic "building blocks" onto massively complex chips, will have astounding implications for electronic design-and the world at large-for decades to come.

The emergence of systems on a chip is being driven by the confluence of several broad technology and market trends. Chip complexity continues to escalate by a factor of 10x every six years and will soon push gate counts into the tens of millions. Cost per gate is simultaneously declining in response to shrinking physical geometries, increasing wafer size, and more fab capacity worldwide. Market demand and the entrepreneurial creation of new ways to satisfy it-particularly in the consumer, communications, and computer segments-contribute to the momentum moving us inexorably toward an era of innovative systems-on-a-chip applications.

Many of the pieces are already in place, but there are still some barriers to break before the goal of systems on a chip can be fully realized. Issues involving established business models, intellectual property ownership and protection, design portability, design tools and methodologies, and standards present all of us with new opportunities for innovation, cooperation, and overall market expansion. Issues and challenges notwithstanding, it is clear that systems on a chip is both the future and the fuel for new products, new markets, and a worldwide consumer connection to new forms of information and entertainment.

*Keynote Address*

# Evolution of Telecom and Multimedia and Their Impact on System Design Requirements

Björn Pehrson
KTH/Teleinformatik, Stockholm, Sweden

## Background

The ongoing industrial transformation, supposedly leading to an information society, includes a convergence of cultures and technologies in traditionally separate areas, in particular: media, telecommunication and computer technologies. The convergence is characterized by traditional products and services disappearing and new innovative services and products often appearing with extremely short life cycles.

A technical basis for this convergence is the digitalization. The means of production in these traditionally separate areas are becoming the same; now based on computing and communications. The rapid pace of technical developments has created a large difference between what is possible and what is routinely used. As a consequence, there is both a strong technology push and a strong market pull driving the development of new services and products. This development has been accelerated by political actions, such as deregulation, which have stimulated competition. The whole of society is affected by this convergence. The turbulent, almost revolutionary, pace of development has already hit many industrial sectors.

One of the most affected areas currently is the telecommunications industry. Telecommmunication services and multimedia are undergoing a transformation from plain old telephony services (POTS) and uniformity to chaos and diversity. Many telecom operators have, much to their surprise, recently become aware that in just a short period of time the traffic in their networks has become dominated by non-telephony traffic. In many cases operators report that more than 80-90% of their traffic now is Internet traffic. This trend is expected to accelerate and make voice traffic increasingly insignificant in comparison to the volume traffic generated by other applications. The traditional service and traffic models for narrowband, point-to-point telephony traffic no longer appropriately describe what is going on in their networks. The telecom industry is literally building systems and networks without knowing much about what they are used for. The North American telephone industry has already reported significant problems in networks attempting to carry long-lasting time Internet traffic when they were designed for session times of the order of 3 minutes in POTS. The traffic characteristics are changing and the demand for network capacity is exploding. Also the business models are changing. Within a year, some European operators expect a demand from their Internet users for up to 1000 times more transatlantic capacity than they have been planning for. Is there a market for them to make money providing this growth of capacity?

New applications and services bring new unknown QoS requirements and new traffic models. We lack equipment to measure the traffic, basic mathematical tools to model and analyze the traffic, and models to synthesize networks from. On the technology push side, the progress in photonics seems to cause a change in the bottleneck to processing power from transmission capacity, thus leading to new systems design criteria. Is the formerly clerly defined road of emerging broadband technologies (Broadband ISDN and ATM) the right way to go when they rely heavily on processing capacity to minimize the use of communication capacity, or should it rather take the opposite course? Together, the new user requirements and the new technological prerequisites bring about a revolution. Therefore, the traditional models and

architectures have to be replaced. Many emerging technologies will have to be replaced before they are successfully launched!

Also computer industry experiences a lot of turbulence, although the spirit is more positive. Will ubiquitous high-performance Computing&Communication take the markets from CD and video players and how much will the network computing paradigm change the PC-market?

In order to understand where the development might lead, and where we would like it to lead, it is important to think ahead in terms of visions: What kind of environment will result and what do we want to have beyond the transition period. We can choose to follow or to lead. On the application side, we need precompetitive cooperation between different actors. While on the technology side, we need to break out from the traditional R&D paths. Both of these changes are challenging since they require both a change in vision and a major reallocation of resources and power.

## A Technical Vision

A reasonable technical vision for the Global Information Infrastructure (GII) or the first decade of the 21st century could be that

- Walls become interactive and connected (at 1-2 Gbit/s) to a global high-performance infrastructure.
- Personal Computing and Communication (C&C) systems are integrated in multimodal wearables, including goggles, providing augmented reality by overlaying information on views of the real world, and providing a billion users with mobile wireless access (at 10-155 Mbit/s) to a high-performance infrastructure.
- Personal software assistants help manage information, provide decision support, etc.
- The High-Performance Infrastructure will include high-performance computing and server facilities and support mobile multicast services with dynamic quality of service requirements, including the necessary real-time properties to support interactive distributed applications.
- Distributed switching of terabit/s of aggregate data flows from connections with dynamic characteristics will be supported.
- The cost of personal multimedia communication will be as low as telephone calls today.

It is evident that not many existing, or even emerging, technologies scale to cope with this vision. GII testbeds should therefore not prescribe any particular technology but allow for experiments at all levels. The issues to be explored include:

- What will future telecommunication systems architectures be? The research community and industry should co-operate in industrial application projects to extract realistic systems requirements as input to research programs.
- How will they be realised? This issue requires interdisciplinary research to study realisation schemes with optimal price / performance ratios, from usage schemes and man-machine interaction, via computing and communication systems, to photonics and wireless component technologies.
- How will we transition to these systems and how will these systems interoperate with legacy systems? Again the research community and industry must interact closely to ensure realistic scaling properties and design migration strategies.

## Discussion

I would like to concretize some of the issues above by discussing a selection of vertically integrated research issues addressing the full range from end-user applications to low-level technical issues and methodology development which we, as part of our Personal Computing and Communication Center, have identified as key issues to make the integration of computing&communication happen.

## Applications and New Service Models

To many technologists, this topic might appear to be of little relevance for core systems design principles. However, knowledge in this area is vital as we have to understand the human factors issues in order to get our systems accepted.

- The 21st Century Applications & Services Model, including QoS and traffic issues: The task of defining a new service model which completely replaces POTS is a truly interdisciplinary issue. It cannot simply be sorted out in research laboratories, but requires pilot systems to be deployed and field tests to be conducted involving real users. The ultimate criteria by which new applications will be judged will probably emphasize quality of life and efficiency of organizations. How (if we could choose freely) would we like to live, both at work and at our leisure? The user requirements will probably emphasize ubiquitous global high-performance mobile access supporting synchronous as well as asynchronous group communication, at no higher cost than telephony services today. Does a technology providing such services exist? Could we adopt it, even if it existed?
- A generic application: Support for meeting processes, a subproblem of CSCW: The importance of this application is to understand to what extent humans can rely on a ubiquitous computing&communication environment. The application should comprise online support for individual meetings which may be either face to face meetings, voice telephone conferences, video conferences, liveboard equipped working group meetings, synchronous computer mediated communications, asynchronous computer mediated meetings; and could involve use of network resources for media-on-demand, etc.
- New experimental applications, such as large Scale Collaborative Distributed Virtual Environments supporting augmented reality: Distributed Virtual Reality (VR) directed towards collaboration provides a service for human cooperation based on 3D. In a distributed VR environment, a shared, interactive 3D world is, in real-time, presented to multiple participants. The technology is currently being developed within the 3D WWW (VRML) standardisation and by the military. Collaboration within distributed VR for a large number (100-1000) of participants within a global scope is currently a research activity, but the technology is being developed with the emergence of the software and hardware infrastructure, including cheap computer hardware and software, group communication protocols, etc. Distributed VR may prove to be the next generation computer interfaces for ubiquitous computing. It will definitely have an impact on electronic conferencing, meetings, entertainment, distributed CAD-based engineering, etc.
- Networked Education - To make the point that the ongoing transformation is profound, I will discuss applications and services from another sector of human society which is in a state of rapid change due to new technology, deregulation and competition: the educational system. It is widely acknowledged as important and often supported by public funds. It also fills a large and growing part of our lives. In one of the possible scenarios, the future education system will become a distributed system, or a "Chaordic" system, according to the Visa model. Educational organizations focus on their strengths and team up in consortia in which there is free competition to contribute the best learning services, part of global exams. The focus is shifting from group teaching to individualized learning, from schedules to just-in-time, etc. The ubiquitous computing & communication concept seems to fit these trends well.

## Systems design issues

- New terminals - wearables? Goggles? Implants? equipped to support location based services? Power consumption?

- Signal processing: Symmetric codec technologies minimizing latency in interactive applications. The current technologies are designed to support storage and retrieval of data rather than interactive services. Improved signal processing for high quality audio, e.g. echo cancelling. The current technologies are designed for telephony quality. Layered compression techniques to support group communication with participants joining via links of different capacity.

- Specialized servers supporting realtime applications in high-speed networks: Traditionally, server computers are general purpose computers designed for high throughput but without consideration of real-time guarantees. Many new applications require real-time responses. e.g. in distributed interactive real-time applications such as distributed virtual reality, video-conferencing, multimedia information systems and video-on-demand. Problems in the software side, regarding the operating system and the applications, should be addressed as well as removing bottlenecks in the host-interface hardware and software by designing new architectures.
- High-performance infrastructure supporting seemless integration of multicast real-time services for high performance distributed computing and for mobile access: The emerging applications often requires real-time and multicast (group communication) services and users would like to have the same services available when they are mobile as when they access the network via a fixed network. Existing protocols are not designed to integrate these services. Dynamic acquisition of terminal addresses, dynamic multicast routing involving seemless handoff of real-time traffic, etc, are all research issues and the solutions are expected to impose new requirements on both software and hardware architectures.
- Switching vs Routing: "Switch when you can and route when you have to" is one of the rules of thumb among todays internetwork designers. By means of concepts like "tag switching" and "IP switching", router designers redefine the meaning of switching and routing in order to remove the processing bottleneck in routers. This will eventually affect the design of switching elements.
- Circuit Switching versus Packet Switching Testbed: Processing capacity is expected to continue to double every 12-18 months over the next decade, which means 100-1000 times more powerful processors by 2006. However, transmission capacity is expected to increase 100 to 1000 or even 10000 times faster due to advances in fibre optics, wavelength division multiplexing, etc.. This evolution suggests that a shift in systems and network design principles, optimising by using less processing and more transmission capacity, might make it possible to provide systems having radically better cost/performance ratios. Going for less processing and more transmission when designing systems and networks might not only simplify the design and manufacturing but also the need for management in the operation phase, which is currently the major cost for telecom operators and it is growing. The shift from traditional telephony networks to broadband integrated services data networks has proven to be much more painful that anticipated due to the complexity of the protocols chosen earlier. Many issues are not resolved, e.g. congestion control. A deeper analysis of the basic design principles might result in a re-evaluation of some of the very basic decisions when moving from circuit-switching to packet/cell-switching. Experimental evaluation of prototypes in testbeds and pilot user experiments are essential.
- Network Management is now the major cost for network operators and its share of the budget seems to increase. The trend towards separate management networks (TMN) should be revaluated focussing on service management issues and the possibility to integrate core network management issues in self-organizing network architectures.
- Network Security: In a time of crises, such as trade sanctions, regional armed conflicts, terrorist actions, organized crime, the survivability of the information infrastructure is essential to the internal security of any society. A future armed conflict will most probably include Information Warfare (IW) aimed at the infrastructure. "Denial of Service" attacks can be expected even in small conflicts, in terrorist actions and even from petty thiefs. Access to the Information Infrastructure can be virtually halted in most countries within hours. There is a need to study and analyse the vulnerability of the Infrastructure against attacks. Develop realistic threat evaluations. Recommend counter-measures and operational procedures. Are smart cards secure enough? Do we want to replace traditional key locks and could we in that case do it reliably enough?

## Design Methodology Issues

- New methods for measuring, modeling and analysis of traffic: Research is needed on new methods for traffic modelling, analysis and control of chaotic/self-similar traffic research on new generation broadband networking monitoring architectures, including identification of attributes, specification of monitoring functionalities needed to support various management functions, investigation of strategies for efficient data recording, storage, and analysis, prototyping and proof of concept.
- Concurrent engineering of hardware and software based on formal methods: The increasing complexity of systems and components call for the use of systematic techniques, efficient use of simulation and design for testability to ensure correctness of designs, as well as methods for performance modeling and analysis, simulation and measurement equipment to optimize performance. The challenge is to find design methodologies that combine correctness and high performance. An even greater challenge might be to find less complex designs doing the same job as the more complex we are working on, and to accept them when we find them. Reducing the complexity, e.g. by reducing processing, might make use of formal techniques more feasible.

## Conclusions

Many traditional truths are being revaluated in the application and systems levels. A few examples have been discussed in this presentation which will most certainly affect the principles for systems design, both from a hardware and a software point of view. It is hard to tell if the cultural or the technical challenge is the greater. In times like this it is important to formulate and discuss longer term visions, not to be caught in short-term dead-ends. Interdisciplinary contact is more important than ever.

# Welcome to ED&TC'97

Welcome to the European Design & Test Conference and Exhibition 1997. It offers you, as did its predecessors, a wide spectrum of interesting activities to choose from: regular paper sessions, poster sessions, tutorials, invited keynotes, panels, hot topics session, User Forum presentations, fringe meetings in the evenings, University Booth in the Exhibition. New activities this year will focus on getting closer to industrial designers in large and small companies: next to the User Forum there will be an industrial Seminar of First Users on Monday and a variety of CAD, design and consultancy activities in several "villages" in the Exhibition area.

The plenary opening session will build further on the presentations of last year. The common thread there was to look at the future consequences in design and test which would result from the implementation of the National Roadmap for Semiconductor Technology of the Semiconductor Industry Association (USA). This year our three invited speakers will take the subject one step further by looking from different perspectives to the future in design and test: Jim Meindl takes a critical view on technology predictions and discusses system design issues from the point of view of physical limitations in semiconductor technology development. Aart de Geus considers in which direction the CAD industry has to move, how it will be affected by the roadmap, what will be its challenges and in which way might these challenges become affordable solutions for industrial designers. Bjorn Pehrson will present a vision on how applications in telecom and multimedia will be able to profit from the process technology advances, how this might enrich out lives and what design challenges it will present. These three different perspectives on the consequences of the IC technology roadmap will influence your own thinking about your future in design and test!

In response to the "Call for Papers" a total of 287 regular papers submissions were received. Hugo De Man and his crew of Topic Chairs and reviewers went through a thorough review process to select 93 paper for oral presentation and 23 for poster presentation. I would like to thank Hugo for his continuing drive for quality and for the excellent organisation, and I would like to thank him for the impressive result which you yourself can check from the Proceedings. Diederik Verkest deserves a special thanks for his efforts to make the first time use of the Web in the review process such a success.

Also the topics chosen this year for Panels and Hot Topic Sessions will certainly evoke your interest. What does it take to transfer successfully advanced design methods and tools to the pragmatic world of qualified industrial design flows? Can conflicts of interest be resolved between the different parties involved in the intellectual property business? What will be the right test methodology for the year 2005? These provoking questions will challenge our panels this year. The Hot Topic sessions will bring you up-to-date with three technical subjects that currently draw much attention: networked CAD systems, deep submicron CAD and multichip packages for consumer applications. The breadth and quality of the people involved convince me that you will not be disappointed in any of these subjects.

Next to all the technical and managerial subjects a major function of any Conference lies in the opportunities it creates for meeting people. This aspect of our Conference has always been given high marks and we continue to pay much attention to it. Coffee breaks, lunches, receptions and fringe meeting are each an excellent opportunity to get into other circles of interest. We will increase the cross-fertilization with the Exhibition by having one of the cocktail parties in the

Exhibition area. We will certainly also maintain the quality of the social event this year and make it into a pleasant souvenir.

Many volunteers have given their best efforts to make this Conference and Exhibition a worthwhile event for all its attendees. I would like to thank the members of the Organising Committee, the Programme Topic Chairs and the reviewers in the Technical Programme Committee, as well as the professional staff from CEP and EDA, for their continued interest and energy in making this the best event of its kind.

**Ludwig D.J. Eggermont**
***General Chair ED&TC'97***

# Tutorials

## A — Formal Verification

*H. Eveking, Technical University Darmstadt, Germany*

*Summary*

There are now two main areas of successful industrial application of formal verification techniques: (a) the verification of large blocks of combinational circuits which is faster and more efficient than simulation techniques, and (b) the checking of equivalence or of temporal properties of finite state systems. Both types of formal verification rely on the efficient representation of boolean functions or large state spaces by means of decision diagrams.

The tutorial will first give an introduction to various types of decision diagrams (OBDD's, OKFDD's, *BMD's). Examples of successful applications of decision diagrams to large blocks of combinational circuits will be presented afterwards. The specific problems of using VHDL as input language will be discussed. Symbolic state space traversal methods allow for the exploration of very large state spaces. The methods can be used to demonstrate the equivalence of two finite state machines or to verify temporal properties by model-checking. In addition, many applications use model-checking as a debugging rather than as a verification tool in order to detect bugs as early as possible and to reduce design time. The tutorial will give an introduction to symbolic state space traversal methods, and will again consider VHDL-related aspects.

## B — Systems-On-Chip: From Design Validation to System Test

*P. Prinetto, Politecnico di Torino, Italy*
*Y. Zorian, LogicVision, USA*

*Summary*

Today's deep-submicron IC technology allows the creation of complex systems on a single die. This new technology necessitates different practices in design, manufacturing and field test. The tutorial will address the testing challenges in system-on-chip and their corresponding solution. For the system-on-chip design stage, the tutorial will cover a number of advanced solutions in design validation, ATPG, and Built-In Self-Test. These solutions are used during the design of individual embedded cores as well as their incorporation into a full systems-on-chip. They are geared towards the typical use of behavioral and RT level hardware descriptions. Following the design stage, the tutorial will address the state-of-the-art requirements for manufacturing and field tests. Here the emphasis is put on software based techniques in fault injection on the VHDL level for reliability and fault coverage purposes; the reuse strategies of the Built-In Self-Test hardware; and finally the requirements to improve in-field reliability and availability by adopting on-line Built-In Self-Test in complex chips. In general, this tutorial will provide an industrial perspective, while covering current practices and it will also reveal the future challenges. Outline:

1. Current Trends in Systems-on-chip Technology
2. Design Validation Solutions
3. High Level Test Generation Concepts
4. Designing self-testable Embedded Cores
5. Testability needs for complete systems-on-chip
6. Fault Injection on VHDL Level
7. In-System Reliability with on-line BIST
8. Future Perspectives

## C — Rapid Prototyping of Digital Signal Processing Systems

*R. Lauwereins, Katholieke Universiteit Leuven, Belgium*

*Summary*

Rapid Prototyping is one of the techniques used to reduce the time-to-market of present day complex Digital Signal Processing Systems. This tutorial aims at presenting the possibilities and limitations of rapid prototyping for application domains ranging from speech processing via audio, image and video processing to telecommunications. It is structured in three parts.

The first part situates prototyping in the product design flow and presents a classification scheme which enables to quickly position rapid prototyping environments and platforms with respect to the type of verification they allow and the supported application domain.

The second part gives an extensive overview of the rapid prototyping environments for digital signal processing systems that are on the market. By including the most advanced research environments, it also offers an outlook to the future capabilities of the commercial tools.

The last part describes one environment that supports heterogeneous targets consisting of multiple processors and Field Programmable Gate Arrays in more detail. The specification model is presented as well as the design flow. Its usefulness is proven by applying the design flow on a toy example and a real-world application, both in the telecommunications domain.

## D — Low Power Circuit Design for Multimedia LSI's

*T. Sakurai, University of Tokyo, Japan*
*T. Kuroda, Toshiba Corp., Japan*

*Summary*

Recently, multimedia LSI's are attracting attention. These LSI's are required to achieve high-performance as well as low-power. This tutorial reviews low-power circuit techniques for CMOS multimedia LSI's.

First, the background and the reason why the low-power is asked for now are summarized to clarify the general constraints together with some of the examples of multimedia LSI's. Next, expressions for CMOS circuit power consumption are described. General guidelines for CMOS logic circuit power reduction are basically three-fold: reducing switching probability, reducing load capacitance and reducing operation voltage. In these, using low supply voltage is the most effective way to reduce power, since the CMOS power consumption depends quadratically on the supply voltage. Low voltage designs, however, essentially suffers from lower speed. Some of the solutions for this problem are discussed including the control of MOSFET threshold voltage.

As to the reduction of the load capacitance, pass-transistor logic circuits are described in more detail including the systhesis methdology. Lastly, it is shown that the low-power design is also essential in solving some of the most stringent problems like noise and electromigration problems in deep submicron LSI designs other than the heat crisis.

## E — Hardware/Software Codesign of Embedded Systems

*J. Henkel, Technical University Braunschweig, Germany*
*F. Vahid, University of California, Riverside, USA*
*L. Ramachandran, LSI Logic Corp., USA*

*Summary*
Hardware/Software Codesign has become a rapidly increasing area of investigation. Codesign techniques permit the design of increasingly complex mided hardware/software systems at a higher level of abstraction than possible with today's tools, which results in a substantial reduction in the economical important time-to-market factor. Furthermore, necessary design techniques like High-Level Synthesis have matured to the point where they can be used in industrial environments, making HW/SW Codesign techniques feasible.

The authors present an overview of the wide area of HW/SW Codesign. After introducing the economically interesting area of embedded systems, they describe current approaches to HW/SW Codesign, discuss algorithms for the key issue of HW/SW partitioning, and present hardware and software synthesis methods, among other subjects.

The tutorial demonstrates how HW/SW Codesign techniques result in the important effects of short turnaround times, reduced time to market and minimized costs. A conclusion discusses today's major problems and suggestions what is needed for an industrial acceptance of HW/SW Codesign.

## F — Built-In Self Test for Embedded Cores

*J. Rajski, Mentor Graphics Corp., USA*

*Summary*
With today's technology, it is possible to build very large systems containing many embedded cores on a single piece of silicon. Since Built-In Self Test (BIST) provides natural embedding of test solutions, it is very effective in dealing with intellectual property, at-speed testing and rapidly increasing size of system ASICs.

The tutorial will introduce state-of-the-art BIST technology, and will discuss its trade-offs, benefits and constraints. It will cover fundamentals of BIST, BIST architectures for logic, memory arrays and processor cores. It will present integration issues in hierarchical BIST solutions for system ASICs, discuss requirements for BIST-ready cores, introduce automation of BIST synthesis. Finally, the tutorial will illustrate applications and discuss future trends of BIST technology.

*Audience*
System ASIC designers, IP providers, test engineers, researchers, and managers interested in learning about state-of-the-art BIST technology, its advantages and limitations, future trends and challenges.

## G — Multimedia Architectures

*N. Demassieux, ENST, Paris, France*
*P. Pirsch, University of Hannover, Germany*

*Summary*
This tutorial addresses the requirements of multimedia on processors and systems. Alternative components and systems for multimedia will be briefly described. The discussion includes platforms such as PCs, set-top boxes, network computers, broadcast coders and professional studios.

For multimedia applications videocoding and decoding have shown the most demanding tasks. They will be identified to explain the computational requirements and their impact on processors. Architectural trends of multimedia-enhanced and multimedia-dedicated processors will be examined. This includes VLIW architectures and super scalar RISC structures.

The tutorial will focus on some key components and present technical details by case studies. Different approaches for processors are explained for consumer markets (TRIMEDIA), personal computers (Intel-MMX), workstations (Sun UltraSPARC) and research projects (HiPAR, PRISMA, PVP). Practical design aspects of dedicated key components will be discussed for the example of an ASIC for motion estimation. The tutorial will conclude with future prospectives by the evolution of architectures (MIMD, super parallelism) and multimedia (real time image synthesis, real-time/real-life virtual reality).

## H — CAD Tools for Analog and Mixed-Signal ASIC Design

*G. Gielen, Katholieke Universiteit Leuven, Belgium*

*Summary*
For reasons of cost and performance the microelectronics industry has always shown a need to integrate more and more functions on a single chip. In recent years, this has resulted in a growing tendency to integrate the analog interface circuits together with the digital signal processing circuitry onto the same IC, leading to true heterogeneous systems on silicon.

The tutorial intends to give an overview of the state of the art in CAD tools for analog and mixed-signal ASIC design. Starting from a description of the general design flow for mixed-signal ASICs, different key aspects will be presented in more detail. The first part of the tutorial will be dedicated to mixed-signal simulation tools, including both mixed-mode and multi-level (including analog behavioral level) capabilities. Also the progress in standardizing analog behavioral description languagues will be discussed.

The second part of the tutorial will be dedicated to analog synthesis and layout tools. Here an overview will be given of the present status of these tools, discussing their capabilities and limitations. Also the problems of physical interactions between analog and digital circuits (e.g. substrate noise) will be described. The tutorial will be illustrated with several practical design examples.

# Best Paper Awards

Each year, the European Design & Test Conference presents awards to the authors of the most outstanding papers. The selection is based on the results of the voting by the participants.

For 1996, the paper selected as the most outstanding in the field of CAD is;

## Gate Sizing: a General Purpose Optimization Approach

*by Olivier Coudert of Synopsys, Inc.*

This paper presents new methods for choosing for each node of a mapped network a gate implementation in the library so that some cost function is optimized under some constraints. Methods for power or/and area optimization under delay constraints or delay optimization under power and/or area constraints are presented.

For 1996, the paper selected by the Committee as the most outstanding in the field of Test is:

## Designing Self-Testable Multi-Chip Modules

*by Yervant Zorian, Hakim Bederr, AT&T*

This paper addresses the problem of Multi-Chip Module (MCM) testing, and specifically testing assembled MCM performance. The presented solution is based on self-test. It augments the conventional single-chip BIST approach, which is needed to produce known-good-dies, to a new multi-chip BIST solution.

## Congratulations to the winners!

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# Networked CAD Systems

Session Chair: Giovanni De Micheli, Stanford University, Stanford, CA, USA

Panellists: David Ku, Escalade Inc.
Luca Benini, Stanford University, Stanford, CA, USA
David Lidsky, U.C. Berkeley, Berkeley, CA, USA

Computer-aided design (CAD) tools have become an essential part in the design flow of any complex electronic system. At the same time, the number of tools needed to implement complex systems is increasing and such tools are generally provided by several suppliers. Integration of CAD tools into unified frameworks prompts for an increasing effort in the creation of standard interfaces. The definition of standard formats for design descriptions such as VHDL and EDIF has been an important milestone in this direction. However, the user interfaces provided by different CAD vendors still lack in uniformity and compatibility.

Moreover design teams are often geographically dispersed, even though they may be working on different parts or facets of the same design. Design reuse of libraries, hard/soft macros, and embedded software may require access to resources that are also geographically dispersed. Fortunately, computer networks such as *intranets* and the *internet* provide pervasive reliable links among designers and design data, as well as an useful means of storing and classifying information. In addition, network browsers and helpers have simplified the access to remote and distributed information, by providing a uniform mechanism which is easy to learn.

The use of computer-aided design tools over intranets and the internet is raising a large interest because of research and business opportunities. Most corporations, where designs are performed at different sites, use intranets for data sharing and communication. Computationally demanding tasks can be performed on high-performance servers remotely connected to the designers by intranet links. Nevertheless, CAD tools are still developed and marketed to be used in specific locations, and the use of intranets to improve upon the design cycle is left to the needs and the ingenuity of the designers.

We expect to see distributed CAD environments for intranets on the market soon. Such environments will make transparent to the designer the location of tools, libraries and design data. This will increase designers' productivity by providing them with uniform access to resources as well as faster response time on computationally-expensive tasks because of load balancing across the network.

The next challenge is to develop distributed CAD environments over the internet. The *world-wide web* (WWW) provides a link to virtually all users of scientific computing and WWW browsers provide *de facto* standard user interfaces. Whereas the WWW has been mainly used until now for information retrieval, a large potential lays in its use for distributed information processing and in leveraging network programming tools.

CAD programs and environments on the WWW can be developed for scientific and/or commercial reasons. The WWW is an ideal means for dissemination of information. Thus, CAD tools developed in academia may be interfaced to the WWW for the purpose of supporting remote access and demonstrations, and providing world-wide exposure. Collaborative research programs at different institutions can use the WWW as a way of interfacing CAD tools. In this perspective, the WWW may play a role similar to the original role of ARPANET.

The commercial opportunities for distributed CAD services are promising as well. New tool usage paradigms may emerge. Designers could temporarily connect to a tool provider, perform a specific task and be billed on a usage-time basis. Design flows may incorporate the use of remotely-located tools, with different costs and objectives, and customizable according to the design goals. CAD vendors may offer free, or limited-cost, tool usage to advertise their products.

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There are clearly many ways of envisioning the development of networked CAD systems on intranets and on the internet. Difficulties may arise due to several factors, including data consistency, network loads, limited bandwidth and response delays. Design of electronic products using the internet must address security problem related to design and technology data. Despite these difficulties, the rapid growth of network-based products and the potential payoffs of networked CAD make this field an exciting area of research.

# Multichip Packages for Consumer Applications

Session Chair: Math Muris, Philips Research/ED&T, The Netherlands

Panellists: Herman Casier, Alcatel Mietec, Brussels, Belgium
Urs Fawer, Philips Semiconductors, Zurich, Switzerland
Wolfgang Radlik, Siemens Research, Munich, Germany
Claudio Truzzi, IMEC, Leuven, Belgium

Application of Multichip Packages is becoming more and more interesting for small-sized, light-weight, cost-sensitive portable consumer equipment. After hearing our panellists on marketing, design, testing, substrates, packages, ppm budgets and KGD issues related to MCPs for consumer applications, we like you to join us in a discussion on the pros and cons of this technology.

Since the dark ages of mainframe computers, Multichip Modules have been used for achieving performance targets which couldn't be met with existing Printed Circuit Board technologies. The high costs for design, manufacturing and test of these Multichip Modules were acceptable for professional applications.

Our bright current age, full of portable multimedia consumer applications, also cries out for Multichip Modules, but now the driving forces are small-sizes, light-weight, low power, combination of technologies, time-to-market and low costs.

Our panelists will introduce you to the issues involved with design, technology, manufacturing and test of Multichip Packages for consumer applications.

Wolfing Readily will give an overview of the current status of substrates and packages for MCPs, with a focus on consumer applications.

Cloud Truss will present MCM-specific design issues concentrating around availability and infrastructure, it's impact on the early stages of design and what strategies are being applied in the US and in Europe to address these issues.

Math Moors will summarize test strategies for obtaining KGDs and MCPs based on underlying requirements for quality and reliability, geared towards cost sensitive consumer products.

Urs Fawer will concentrate on design experiences (constraints from sub-contractor/customer, lead time, "design-flow"), examples and ad-hoc solutions.

Herman Casier will take the position that MCPs will only provide a temporary solution, because high volume demands will always lead to a dedicated IC technology, resulting in a single die solution.

Following these introductions, the audience is invited to discuss with the panel the pros and cons of this MCP technology.

# Deep Submicron CAD

Session Chair: Ralph Otten, Delft University of Technology, Delft, The Netherlands

Panellists: Keith Baker, Philips Research, Eindhoven, The Netherlands
Raul Camposano, Synopsys Inc., Mountain View, CA USA
Antun Domic, Cadence Design Systems Inc., San Jose, CA, USA
Patrick Groeneveld, Compass Design Automation, San Jose, CA, USA

As microstrip features scale into regimes of close to or below a tenth of a micron new metrics obtain importance beside the traditional area, time and power objectives.
A decade of analysis has shown the increasing effect that interconnect is going to have,
as VLSI systems are effectively transformed into microwave circuits of unprecedented complexity. Not only delay requires a totally new approach, future design systems have to be able to prevent detriments caused by crosstalk and resistive voltage drop in an essentially three-dimensional configuration.

The return on investment of the new technologies will be very disappointing when these effects can only be controlled by large safety margins.
This implies that noise immunity is going to be one of the new metrics to enter the field and will extort compromises with timing and area demands.

Also, whatever the solutions are going to be, how will they affect the robustness of layout, and finally, how do we find out efficiently whether the circuit should pass the test stages.

It is clear to everybody that the interplay of different stages in design is going to become more intensive, even so that no longer layout design, logic synthesis and higher levels of synthesis can be treated sequentially or even iteratively. A complete integration into what already has been coined the design planning approach will be mandatory.

The questions that are going to be tackled in this session are:

- How are the new metrics going to be incorporated into the tools for designing these so-called deep-submicron circuits?
- How is one to retain the relative design comfort of the digital abstraction?
- What are the test methodologies going to be like for this new generation of VLSI circuits?
- How are the upto now separate design stages to be integrated in the design plan?
- Will vendors be capable to develop the right tools far from where technology is being developed, or is this going to be the exclusive terrain of corporate CAD?
- And is university research going to have a place in it after it had such a significant contribution to the development of analysis for three-dimensional deep submicron structures?

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# Panel Session

## How to Introduce Advanced Design Technology in Qualified Industrial Design Flows ?

Moderator

Patrick De Wilde, DIMES, The Netherlands

Participants

Philippe Reynaert, Mentor Graphics, Belgium
Patrick Pype, CoWare, USA
Rajeev Jain, UCLA, USA
Patrick Odent, Philips, Belgium
Pierre Paulin, ST, France
Kari-Pekka Estola, Nokia, Finland
Henri Cloetens, Philips, Belgium

Time-to-market is a prominent part of most EDA vendor's (and researcher's) sales literature. Although all EDA users say that it is high on their priority list, they seldomly stroke a check on its behalf. One of the reasons is that the benefit of EDA innovation and new methodologies is hard to measure in terms of credible dollar values. Although soft decisions may play a role in the decision process, they don't earn a spot in the spreadsheets. During their decision process, EDA users evaluate more whether a new acquisition fits in their current approach rather than what possible pay-off a new methodology can bring. This leads to the typical process of benchmarking , reference checking, evaluation on different platforms etc. Nevertheless, the importance of methodology cannot be overstated. A methodology that lowers cost, leverages design flow and employs leading edge technology conveys a real competitive advantage. The problem is that it is too hard to quantify, too vague to spend money on and too simple to guide decisions. This panel wants to confront the opinion of researchers, vendors and users on this topic.

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# Panel Session

## Are There Conflicts of Interest in IP Based Business?

Moderator

Marco Cecchini, OMI, CEC

Participants

Julio Goria, Italtel, Italy
Mike Muller, ARM, UK
Rudi Lannoo, Alcatel-Mietec, Belgium
Andreas Wild, Motorola, USA
Oz Levia, Cadence, USA
Brian Barrera, Mentor Graphics, USA

The shift in chip design methodology towards the re-use of virtual components that can contain complex Intellectual Property (IP) requires a cooperation between EDA, semiconductor, systems and (fabless) IP-vendors. This implies a new business model that has to reconcile the, sometimes conflicting, goals of all these players. Semiconductor vendors prefer to lock-in designers to their poprietary processing technology by means of sophisticated libraries. Fabless IP-vendors prefer to license their technology to as many foundries as possible. Systems houses would like to plug and play with IP-components from various sources and make use of a customised design environment that combines the best of breed design tools. Finally, the EDA vendors are making their design environment as attractive as possible by providing as much as possible access to a wide variety of IP components. Moreover it is not always clear how the responsibilities in the design process are shared by all these partners. In case of design failure, is it because of the wrong model of the IP-component, because of the inconsistency between specification and implementation, because of incomplete documentation, because of wrong assumptions made in the design environment. Will standardisation such as the Virtual Socket Interface be the solution to all problems? This panel will discuss the point of view of all the above players in the IP-business.

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# Panel Session

## What Will Be the Right Test Methodology for the Year 2005?

Moderator

Keith Baker, Philips, The Netherlands

Participants

Birger Schneider, Microlex, Denmark
Piet De Pauw, Alcatel-Mietec, Belgium
Tom Williams, IBM, USA
Bob Grubel, TI, USA
Steven Athan, Univ. Florida, USA

Each year the complexity of VLSI systems increases and test development consumes a major portion of the development cycle. The goal of this panel is to discuss the roads that will get test methods into the future. Questions that have to be answered are : what will be the key problems when evolving towards deep-submicron testing , what will be the impact of high level design and synthesis techniques on test issues, how will we cope with systems on silicon combining hardware/software and digital/analog, how will a system test strategy cope with the combination of heterogeneous test approaches (such as Iddq, Bist, Scan) for the different components on a single chip, how can the quality of the test process be improved for devices of more than hundred million transistors. The result of this panel should help the universities and research institutes to identify what will be the requirements of leading (and bleading) edge industrial applications for the year 2000.

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