A Two-dimensional Transistor Placement for Cell Synthesis

Shunji Saika*, Masahiro Fukui, Noriko Shinomiya, Toshiro Akino
Semiconductor Research Center
Matsusita Electric Industrial Co., Ltd.
Moriguchi, Osaka, 570 Japan
saika@vdrl.src.mei.co.jp
Phone : 06 - 906 - 5064
Fax : 06 - 906 - 1406

Abstract

This paper proposes a transistor placement algorithm to generate standard cell layout in a two-dimensional placement style that is not restricted to row-based transistor placement. The cost function constructed for transistor placement optimization is able to optimize wirings directly and diffusion sharing indirectly but sufficiently. This transistor placement algorithm, applied to several standard cells, has demonstrated the capability to generate a nearly optimal two-dimensional placement that is comparable to maually designed placement.

I. Introduction

Semiconductor process technology has made a rapid progress. The development of a high performance LSI based on state-of-the-art process technology requires preparation of a new cell library as soon as possible. And the cell library must meet a variety of demands for LSI systems, such as high performance or low power consumption. In fact, a rapid succession of cell library preparation has occurred in recent years, and each of libraries requires a many kinds of cells. Problems encountered by cell library designers have become more and more difficult as the design rules in this deep sub-micron era increase in complexity.

Almost all layout designs of cells have been made manually. This is because the size of leaf cells directly influences the size of blocks and chips. In the near future, however, manual design will not be able to meet the demands of making the cell libraries in shorter turn-around times. Therefore cell layout synthesis will soon become a critical technology.

We are now developing a cell synthesis program package. Cell layout synthesis, hereafter referred to as "cell synthesis," is the design automation problem of generating layout mask geometries for cells from their transistor-level netlists by applying a certain design rule. It can generally be divided into three sub-problems: (1) transistor placement, (2) routing of internal nets, and (3) compaction. As an approach to the first sub-problem, this paper describes in detail a new transistor placement algorithm.

Many elaborate studies have been presented on the transistor placement problem[1,2,3,4,5,6,7,8,9]. The study by Uehara et al.[1], which proposed layout area reduction by diffusion sharing between adjacent transistors, attracted considerable attention and spurred many kinds of algorithms that maximize diffusion sharing in conjunction with the paring problem between N-transistors and P-transistors. These algorithms are based on one-dimensional layout style. One-dimensional placement involves a row of P-transistors and a row of N-transistors, each row usually being horizontal, and all transistors having the same posture so that the gate width can be expanded vertically.

Even for one cell library series, various types of cells must be prepared, from high-speed respoding types to power-saving ones, so transistor sizes varies greatly, depneding on cell types. Accordingly, when the cell height is fixed, as is usually the case in a standard cell library, one-dimensional layout generally fails to achieve the optimum layout that ca be gained gained by manual design.

Some two-dimensional transistor placements have been previously proposed [6], but almost all of them realize two-dimensional placement simply by iterating one-dimensional placements vertically. Such two-dimensional approaches would be effective for macro cells rather than for standard cells.

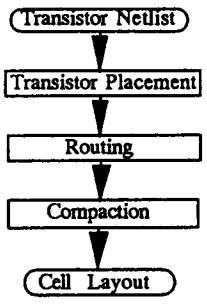

Fig.1 cell synthesis flow

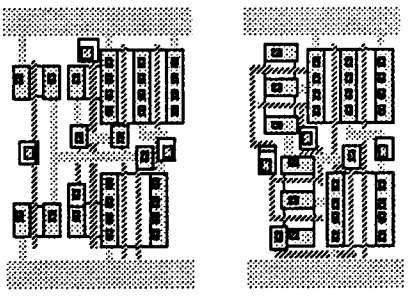

Fig.2 one-dimensional layout and two-dimensional layout

ASP-DAC '97
0-89791-851-7$5.00

The SOLO[7] system can generate a kind of fully two-dimensional layout for leaf cells, but this method divides the cell into partial circuits and then applies specific geometries -- the gate matrix model -- to each of the partial circuits, so the cell itself is not necessarily optimized. In addition, the cell layout produced by the SOLO seems to be inappropriate for conventional standard cell design style where two channels of P and N are clearly separated in a cell.

Fig.2 shows an example of the difference between one-dimensional design and manual design. Manual design allows transistors in each channel to range not only horizontally but also vertically with any of the two postures of vertical gate and horizontal gate. Here, we call such manual design "the two-dimensional placement style". This paper and proposes a new transistor placement algorithm oriented to the two-dimensional style.

II. Approach

To apply transistor placement and cell synthesis to a practical way of generating standard cells, we assume unconstrained general CMOS circuits that could include some transfer gates or an unequal number of P and N transistors. Taking in a transistor level netlist that describes the internal connections between transistors in the circuit and the sizes of the transistors, the transistor placement determines the positions and orientations of every transistor. In the output from the transistor placement, all transistors are assigned to diffusion islands, and in each island transistors are aligned in one direction seperated from adjacent transistors according to the design rule used. The islands themselves are placed in the manner of two-dimensional stlye, seperated from each other depending on rough estimations of wire densities. Through our cell synthesis, a kind of symbolic router and a compaction follow the transistor placement, so we can eventually obtain the layout mask geometries for cells that satisfy the constraints of the design rules.

As for cell model, we assume a general design style of standard cells. In the cell model, the power bus and ground bus are horizontally located at the top and bottom of the cell respectively. The upper half of the cell is P-channel area and the lower N-channel area. We call a transistor "a vertically placed transistor" if its gate width is vertical and "a horizontally placed transistor" if its gate width is horizontal. The cell height, each channel's height, and the power and ground bus width are fixed. The locations of input/output pins are not fixed.

The first sub-task of transistor placement is to generate groups of transistors. Although an efficient set of groups serves greatly to simplify the transistor placement task by introducing a placement hierarchy, it is difficult to generate such an efficient set of groups in the case of general CMOS circuits. If the average number of transistors in a group is larger, then the efficiency of simplifying the task of group placement is clearly higher. On the other hand, if the choices of transistor placement in a group increase, the intra-group placement obtained may not be the best due to the placement of the groups. Conventional tactics of generating groups involves either gathering the transistors in a group recognized as being in a logic gate, aligning a P-transistor and a N-transistor with gates to be connected to each other, or constructing diffusion islands maximizing diffusion sharing. These tactics are generally believed effective for transistor placement problems, but they neither necessarily give one solution nor robustly ensure the best final transistor placement. We use a set of groups that is simply made but effective to avoid concern about th quality of the set of groups. In fact, we simply gather transistors in a series into a group.

The second sub-task of transistor placement is to place the groups in a one-dimensional style. The cell height for a standard cell library is predetermined to accommodate vertically placed transistors with a standard gate width in the library. The greater part of manually designed cells take one-dimesional style in which transistors are all vertically placed and diffusion islands are all horizontal rows. Although we employ two-dimensional style in the final placement, we first optimize group placement first in the one-dimesional style. Because this one-dimensional placement serves as preparation for the subsequent two-dimesional placement, its objective is to provide the placement best capable of being optimized for final placement in two-dimensional style. For this purpose, we first consider the wires between transistors for the potential of expansion to two-dimesional style and secondly consider the transistor chaining for the cell width. In the one-dimensional placement optimizaton, the cost function we adopt is the total estimation of the net extents that comprises four part of extent estimation for each net. With this cost function, it is important that the positions of all of the transistors be estimated in such an accurate manner that the positions satisfy the seperation rules between adjacent transistors, which depend on whether the two transistors share a common diffusion. The cost function calculated with sufficient accuracy can optimize the net extent directly and the cell width indirectly in one-dimensional placement.

Before two-dimensional placement optimization, the third sub-task of transistor placement is to fold transistors that are relatively large. To generate cell layout satisfying the cell height restriction, transistors that are too large in their gate width must be folded so that the new transistors generated after the folding are able to stand vertically in their channel area. Because we fold transistors after the one-dimensional placement, we can take into account the wire density estimated in the one-dimensional placement and then fold the transistors effectively.

The final sub-task of transistor placement is to generate transistor placement in the two-dimensional placement style. In this phase, the transistor placement exploits the high flexibility of two-dimensional style to locally improve the result of one-dimensional placement and finally obtain the optimal two-dimensional transistor placement. The pre-

optimization in one-dimesional placement is advantageous as it is suited to the design style of the standard cell, which is fixed in height and can thus change its dimension only in width. If the cell contains a transistor whose size is not suited to one-dimensional layout, which is relatively narrow, it is handled well in the local improvement step of the two-dimensional placement to realize a layout of sufficient integration density.

III. Placement Algorithm

A. Group Generation

When a set of transistors is called a transistor series, this means that every net representing any internal connection in the set, with no more connectons to external transistors, consists of just two diffusion terminals. When a set of transistors is called a maximum transistor series, this means that the set is a transistor series that cannot support the addition of any more transistors. Transistors are grouped so that for every maximum transistor series, all the transistors in it are collected into a group. No more than two maximum series are ever collected into a group. After this grouping based on transistor series, every transistor that is not yet grouped is treated as a group, and the group becomes a single-transistor group. In Fig.3, there are four groups that each include two or more transistors, and the rest of the transistors represent single-transistor groups. A net representing a group's internal connection is independent from the transistors in other groups. Therefore, a group can be placed on a diffusion island that does not require contact at any intermediate diffusion node. In addition, it is expected that transistors within a series have the same size and the diffusion island can be rectangular without protrusion or recess. The contact-less rectangular diffusion island's geometry is clearly the best layout for a group. It is essential for our transistor placement algorithm that none of the groups be so large as to affect the overall placement optimization for the cell.

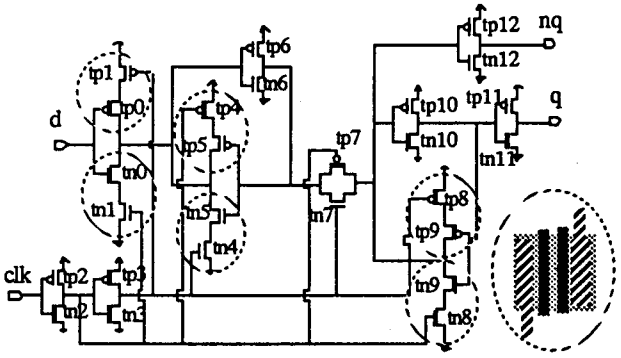

Fig.3 example flip-flop circuit and groups

B. One-Dimensional Placement Optimization

The one-dimensional optimization starts with an arbitrary initial layout and performs iterative improvements using the simulated annealing algorithm.

< One-Dimensional Placement Model >

An example of the one-dimensional lattice model we use is shown in Fig.4. The lattice points range horizontally, and each lattice point may have at most one P-transistor and one N-transistor vertically placed. There may be points with no transistor assigned. The number of lattice points may be any integer not less than the maximum between the number of P-transistors and that of N-transistors. As the number of lattice points increases, the space for placement configurations becomes larger. However, some margin against the number of transistors brings an effect of increasing the number of optimal configurations in the space of feasible ones. We know from experiments that it is a good strategy to let the number of lattice points be given a relatively large rate margin based on the the maximum between the number of P-transistors and that of N-transistors. For example, in a problem including 13 P-transistors and the same number of N-transistors, a good optimization performs on a lattice model of 18 lattice points with a margin of 5 given. Ascending integer numbers, starting with zero, are given to the lattice points from the left and represent the lattice coordinates. The lattice coordinate of each transistor is defined as that of the point it belongs to.

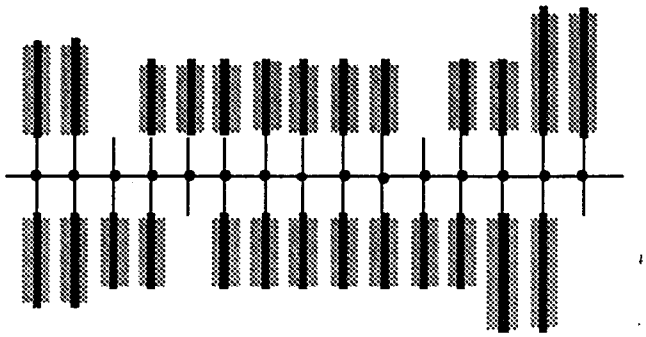

Fig.4 one-dimensional placement model

< Placement of Groups >

All of the groups, including single-transistor groups, are the one-dimesional placement elements. As is mentioned above, a group consists of a series of transistors and the fixed geometry of a group is a contact-less rectangular diffusion island. Accordingly, a group of transistors is placed on the lattice model to occupy a series of points. A signal flow can be defined in a group that goes into one of the edge transistors of the group and out of the other. In the fixed island geometry of a group on the one-dimensional lattice model, the transistors are arnaged along the singnal flow either from left to right or from right to left. This shows that a group can be placed in the two figures on the one-dimensional lattice model. Therefore,

we define the original figure of a group, a fixed diffusion island, so that the signal flow defined for the group goes from right to left. The transistor that the signal flow goes out of is defined as the original transistor of the group, while the lattice coordinate of the original transistor is defined as the original lattice coordinate of the group. Against the original figure of a group, another figure is obtained by fliping the group around the vertical y-axis. In the one-dimensional placement optimization, modifying a placement configuration means changing the original lattice point of a group or to flip a group.

< Generation of New Placement Configuration >

We prepared three types of moves that can be used to modify a current placement configuration.

FLIP: flip a group around the y-axis, keeping the set of lattice points occupied by the group
JUMP: change the original lattice of a group
EXCHANGE: swap a pair of groups

A FLIP move is to flip a group and exchange its figure. If the transistors of the group are arranged from right to left, the arrangement will be from left to right after the FLIP move operation and vice versa. The original lattice point of the group is changed so that the area occupied by the group on the lattice model does not move. A JUMP move changes the original lattice point of a group. When a new point is designated, the group is moved and placed at the new original lattice point. If there is not enough successive empty points to be occupied around the new point, other groups lying between the current original point and the new point are slid to ensure the necessary space for the group under this operation. An EXCHANGE exchanges the original points of a pair of two groups. If the numbers of transistors of the two groups are different, there might not be enough space around the new point. In that case, other groups between the two groups are slid to ensure space, as in the case of JUMP.

At each step of modification, we select one among the three types of moves by using a series of random numbers ranging from 0 to 1. This selection requires us to define the probability of appearance for each type of move. The set of probabilities we use is

$$P(\text{FLIP}) = 0.1,\ P(\text{JUMP}) = 0.45,\ P(\text{EXCHANGE}) = 0.45$$

at each stage of temperature. At the end of annealing, we apply a greedy algorithm using the following set of probabilities :

$$P(\text{FLIP}) = 0.4,\ P(\text{JUMP}) = 0.3,\ P(\text{EXCHANGE}) = 0.3$$

In addition, we adopt a limit of moving distance for JUMP and EXCHANGE moves. Represented in the rate to the whole number of lattice points, the limits in annealing phase and in greedy phase are

$$LT(\text{in annealing}) = 0.6,\ LT(\text{in greedy}) = 0.2.$$

< Cost Function >

Each placement configuration is evaluated by net extent. Evaluated net must be a signal net and a net between two groups; power net and ground net are not included. Input/output related nets are included.

Each of the transistor level nets consists of diffusion terminals for source and drain as well as gate terminals. A net can be separated into the three parts of terminals: P-diffusion terminals, N-diffusion terminals and gate terminals. It is possible to consider the four types of extent for each net: (1) extent of P-diffusion terminals, (2) extent of N-diffusion terminals, (3) extent of gate terminals, and (4) whole extent of all the terminals. For one-dimensional placement, the net extent is evaluated only in the horizontal direction. The extent of each type is defined as the horizontal distance between the left-most and the right-most terminal elements.

To evaluate a placement configuration effectively, it is necessary to foresee the mask geometies from the configuration on the lattice model. Therefore, the four extents should be evaluated after estimating the positions of transistors according to the design rules. The estimation of positions can be performed by simultaneously scanning both the P and N rows of transistors from left to right on the one-dimensional lattice model. If a pair of adjacent diffusion terminals belong to the same net, the distance between the pair of transistors follows the design rule for diffusion sharing. If not, the design rule for diffusion separation is applied. In addition, within the same group no contacts are required, but if two groups are connected to each other through diffusion sharing, there must be contacts. Thus, for diffusion sharing, distance evaluation differs between intra-group and inter-group values. When the positions of transistors are estimated with consideration to the differences in distance between a pair of adjacent transistors, the current situation of diffusion sharing in the cell is reflected in the value of net extent. Therefore, our cost function described below, although based on the evaluation of net extent, can optimize indirectly the transistor chaining that directly represents cell width.

Sometimes the numbers of P-channel and N-channel transistors are much different, and there are many empty lattice points for a smaller transistor area. It is wrong, however, to eliminate such empty points without any reason by moving transistors to the left as far as possible. In our algorithm, if there are empty points between transistors, before determining the transistor position immediately adjacent to the empty point the configuration of the other channel is referenced to avoid such a wrong move.

After these preparations, we define a placement evaluation function, which is the cost function. Let S be the evaluation function. For the four types of net extent, let A be the extent of P-diffusion terminals, B be the extent of N-diffusion terminals, C be the extent of gate terminals and D be the extent of all terminals. Now our cost function S is

$$S = W1 * A + W2 * B + W3 * C + W4 * D$$

where W1, W2, W3 and W4 are weight constants. If we set these weights as

$$W1 = 0,\ W2 = 0,\ W3 = 0,\ W4 = 1.0,$$

the cost function represents the conventional wire length estimation.

In S, the part of (W1 * A) functions to allow the P-diffusion terminals come to near each other; in the best possible cases, overlapping occurs through diffusion sharing. The second part of (W2 * B) functions for the N-diffusion terminals in the same manner as the first part does for the P-diffusion terminals. The third part of (W3 * C) is apparently to align the PS gate terminals, especially for a pair of two P and N transistors. The last part of S is (W4 * D), which simply reduces the total wire length in the cell.

We use a set of values of W1, W2, W3 and W4 as follows.

$$W1 = 0.5,\ W2 = 0.5,\ W3 = 0.5,\ W4 = 1.0$$

C. Transistor Folding

In this step, we first estimate the width of vertical space for transistor placement remaining in the cell while considering the density of horizontal wiring given by the one-dimensional transistor placement result. While a part of the polysilicon wiring can be placed on the power line at the top of the cell or on the ground line at the bottom, metal wiring is concentrated at the middle of the cell. The height of the area remaining for transistors can be estimated by evenly distributing the height occupied by metal wiring to p-channel and n-channel areas and subtracting the wiring height from each channel's height given by the rules for the standard cell.

The acceptable gate width of a transistor depends on its location in the cell because the wiring density varies depending on the transistor placement configuration. If this fact is ignored and transistors are simply folded according to the channel height given by the cell design rule, there is no assurance that the layout can be completed within the cell height. Our algorithm, in which transistors are folded by utilizing the estimation of transistor area height based on wire density, obtains the best size for any given cell height.

D. Two-dimensional Placement Optimization

The one-dimensional placement is expanded into two-dimensional placement in this step. If two-dimensional placement is not necessary, a one-dimensional layout can be refined in this step to meet the needs of an actual layout.

The two-dimensional lattice model is defined as in the same way for the one-dimensional model. This model assigns transistors to the lattice points. A transistor is placed on the lattice plane as a line segment with a direction and a length. The length represents the width of the transistor's gate. A transistor generally occupies a straight line segment consisting of multiple lattice points.

A lattice point has its actual vertical and horizontal size and distance to the next points. The actual size of a lattice point is determined by the assigned elements, which are the transistor and wires, and the actual distance between lattice points is determined by the design rules of the assigned elements, which also reflect the sharing status of the adjacent diffusions.

The two-dimensional optimizaton uses the iterative improvements from the simulated annealing algorithm and conducts a local optimization at low temperature. The purpose of two-dimensional layout is to locally improve the result of the one-dimensional placement, thus filling unoccupied areas.

Wiring is optimized using the wiring length as the cost function. The wiring structure is assumed to be the same one used in the one-dimensional placement, but the vertical component of a polysilicon path is added to the evaluation objects. The vertical component should be considered because it is desirable to place the gates of equal potential close to each other in a two-dimensional layout. The change of horizontal wiring density is calculated because it is always necessary to examine whether the layout height is within the cell height when optimizing the wiring length. This optimization is conducted under the condition that the layout can be placed in the cell.

IV. Experimental Results

We have implemented this transistor placement system in C program and ran it on the PanaStation SS20.

Fig.5 shows a one-dimesional placement for an exmaple of D-flip-flop including 13 P-transistors and the same number of N-transistors. Fig.6 shows a two-dimesional placement for the same cell, following the one-dimensional placement of Fig.5. In both layouts, wiring is performed by hand, but the cost cannot be influenced by wiring paths. This example of one-dimensional placement produces a cost that is far from optimal. In the two-dimensional optimization, cost decreases from 4240 to 3905, with cell width decreasing about 33%. But the cell height in Fig.6 is larger than the height of constraint by 14%. This is due to the immaturity of the two-dimesional placement program.

Fig.7 and Fig.8 represent experimental results of the one-dimensional placement for an example of D-flip-flop that is the same as above and for an example of Set-Reset-D-flip-flop having 19 P-transistors and the same number of N-transistors. These data were obtained by performing a near-optimal annealing. It can be seen that these one-dimensional placement results closely match the optimal one-dimensional placements.

V. Conclusion

A two-dimensional transistor placement algorithm for standard cell layout synthesis is proposed. This transistor placement algorithm in the first stage optimizes the one-

dimesional placement, in the second stage folds the large transistors, and in the final stage optimizes the two-dimensional placement. From the experimental results, our new cost function based on net extent appears to closely match the performance of total optimization flow.

ACKNOWLEDGEMENT

The authers would like to thank Director Takemoto and Dr. Kuninobu of Semiconductor Research Center for their supporting and encouraging our research.

REFERENCES

[1] T. Uehara and W.M. VanCleemput, "Optimal Layout of CMOS functional arrays," IEEE Trans. Computer vol.-30, pp. 305-312, May 1981.

[2] R.L.Maziasz, J.P.Hayes, "Layout Optimization of Static CMOS Functional Cells," IEEE Trans. On CAD, vol.9, No.7, July 1990.

[3] S. Wimer, et al., "Optimal Chaining of CMOS Transistors in a Functional Cell," IEEE Trans. CAD, Vol. CAD-6, No. 5, Sep. 1987.

[4] S.Rekhi, J.D.Trotter, D.H.Linder, "Automatic Layout Synthesis of Leaf Cells," DAC, pp.267 - 272, 1995.

[5] M.Lefebvre, C.Chan and G.Martin, "Transistor Placement and Interconnect Algorithms for Leaf Cell Synthesis," EDAC, pp.119 - 123, 1990

[6] K.Tani, K.Izumi, M.Kashimura, et al., "Two Dimensional Layout Synthesis for Large-Scale CMOS Circuits," ICCAD, pp.490 - 493, 1991

[7] D.G.Baltus, J.Allen, "SOLO: A Generator of Efficient Layouts From Optimized MOS Circuit Schematics," DAC, pp.445 - 452, 1988.

[8] Y.Shiraishi, J.Sakemi, M.Kutsuwada, A.Tsukizoe, T.Satoh, "A High Packing Density Module Generator for CMOS Logic Cells," DAC, pp.439 - 444, 1988.

[9] T.Sadakane, H.Nakao, M.Terai, "A New Hierarchical Algorithm for Transistor Placement in COMS Macro Cell Design," CICC, pp.461 - 464, 1995.

[10] M. Fukui and T. Akino, "An Algorithm for VLSI Leaf Cell Generation," VLSI Design Tech., Report VLD94-65, Oct. 1994.(in Japanese)

[11] M. Fukui, N.Shinomiyam and T. Akino, "A New Layout Synthesis for Leaf Cell Design," ASP-DAC, pp.259 - 264, 1995

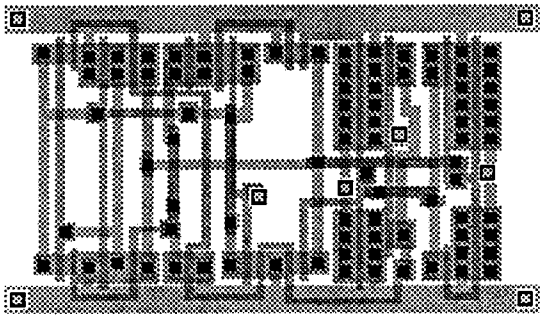

Fig.5 one-dimensional layout

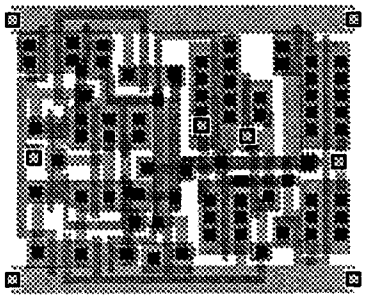

Fig.6 two-dimensional layout

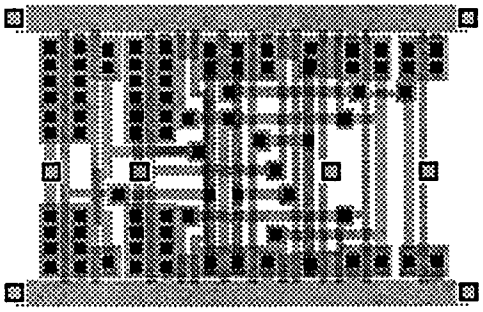

Fig.7 one-dimensional layout for D-flip-flop

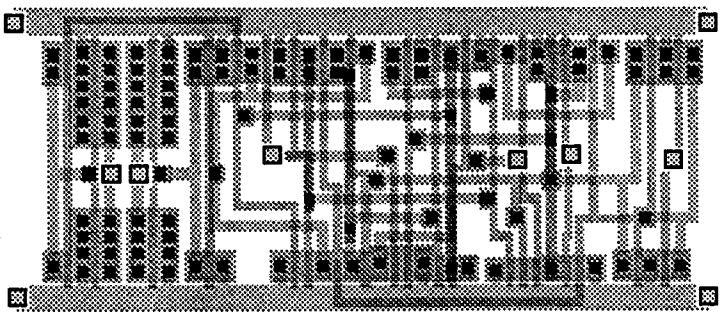

Fig.8 one-dimensional layout for set-reset-D-flip-flop