±1.5V CMOS Four-Quadrant Multiplier

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Abstract – A low-voltage CMOS four-quadrant analogue multiplier using two NMOS operated in the triode region with modified bi-directional regulated cascade (RGC) structure is presented. The circuit can operate from a supply voltage of ±1.5V. For a differential input voltage range up to ±0.8V, this circuit has kept nonlinearity below 0.9% and total harmonic distortion less than 1%. The –3dB bandwidth of this multiplier is 15MHz. The chip was fabricated in Taiwan Semiconductor Manufacturing Corporation (TSMC) 0.8μm Single-Poly-Double-Metal (SPDM) N-well process. The chip dissipates 24.4mW and occupies 251x653μm^2 active area.

I. INTRODUCTION

Analogue four-quadrant multipliers find many applications in modern analogue VLSI signal and information processing; they are required for modulation/demodulation, frequency translation, rectification, signal level compression/expansion (the so called compandor), etc. Multipliers perform nonlinear operations on continuous-valued analog signals. To operate with low supply is becoming a main trend in future development of low power communication IC. Conventional design technique for a CMOS analogue multiplier circuit is based on the square-law characteristics of an MOS transistor [1] –[4]. A Gillert multiplier cell [5] is first introduced in a bipolar technology, and a modified CMOS version of it is also described [6]; however, its power supply can not be properly fitted into low voltage (≤ 3V) range. Few four-quadrant multipliers suitable for low supply voltages are presented in literatures [7] –[11]. Most reported four-quadrant low voltage analog multipliers used cascaded differential input circuit to obtain larger output swing, but the architectures of the multipliers turned out to be more complicated. In this paper, a much simpler configuration that uses only two triode NMOS transistors with the modified bi-directional regulated cascade structure (RGC) [7], [10], [11] consisting of three stages of unity-gain buffer to implement the multiplier is proposed.

II. DESCRIPTION OF MULTIPLIER

Fig. 1 shows the proposed low voltage CMOS four-quadrant multipliers, based on the modified bi-directional RGC structure. It consists of three unity-gain buffers and two NMOS transistors (i.e. N7 and N8) biased in the triode region mainly. The bias circuit is formed by MP1, MP2 and MN2.

The drain current I_D for an NMOS transistor in the triode region can be give n as

$$I_D = \frac{K}{2}[2(V_{GS}-V_{tn})V_{DS}-V_{DS}^2](1+\lambda V_{DS}) \quad (1)$$

where $K = \mu_o C_{ox} W/L$ is transconductance parameter, V_{tn} is threshold voltage, and λ is channel-modulation coefficient.

Four transistors PA1, P4, N1, and NB1 comprise a unity-gain buffer is shown in Fig. 1. The negative feedback from P4 to N1 is used to set N1 in the constant current mode. The currents in PA_i and NB_i (for i = 1 to 3) are biased to be I_{PA} and I_{NB}, respectively. In order that output current will flow through R_L, I_{PA} must be kept below I_{NB}. V_G is adjustable bias voltage for operating N7 and N8 in the triode region. The principle of operation of CMOS four-quadrant multiplier can be derived as follows:

$$I_{PA} = [(V_1 - V_D) - V_{tn}]^2 \frac{K}{2} = [(V_2 - V_S) - V_{tn}]^2 \frac{K}{2} \quad (2)$$

From eqn.(2), it can be shown

$$V_1 - V_D = \sqrt{\frac{2I_{PA}}{K}} + V_{tn} \quad (3)$$

$$V_2 - V_S = \sqrt{\frac{2I_{PA}}{K}} + V_{tn} \quad (4)$$

Since eqn.(3) = eqn.(4), then

$$V_1 - V_D = V_2 - V_S$$

$$V_D - V_S = V_1 - V_2 \quad (5)$$

where voltages V_D and V_S are drain and source voltages for transistor N7 and N8, respectively. Hence, the drain-source voltage is equal to the difference between V_1 and V_2. The voltages V_D and V_S can be given as

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$$V_D = V_D(\text{NB1}) = V_D(\text{NB3}) \quad \text{and} \quad V_S = V_D(\text{NB2})$$

The drain currents of N7 and N8 can be rewritten as

$$I_D(\text{N7}) \cong \frac{K'}{2}[2((V_G + V_3) - V_S - V_{tn})V_{DS} - V_{DS}^2]$$

$$I_D(\text{N8}) \cong \frac{K'}{2}[2((V_G + V_4) - V_S - V_{tn})V_{DS} - V_{DS}^2]$$

where $V_{DS} = V_D - V_S$.

The difference between the drain currents of N7 and N8 will be proportional to the product of the drain-source voltage and the difference of their gate voltage. The differential output current can be then given as

$$I_D(\text{N7}) - I_D(\text{N8}) = K'(V_3 - V_4)(V_D - V_S) \tag{6}$$

where K' is the transconductance parameter of N7 and N8. The difference output voltage V_O of the multiplier can be expressed as

$$\begin{aligned} V_o &= V_{o1} - V_{o2} = [I_D(\text{N7}) - I_D(\text{N8})]R_L \\ &= K'R_L(V_3 - V_4)(V_1 - V_2) \end{aligned} \tag{7}$$

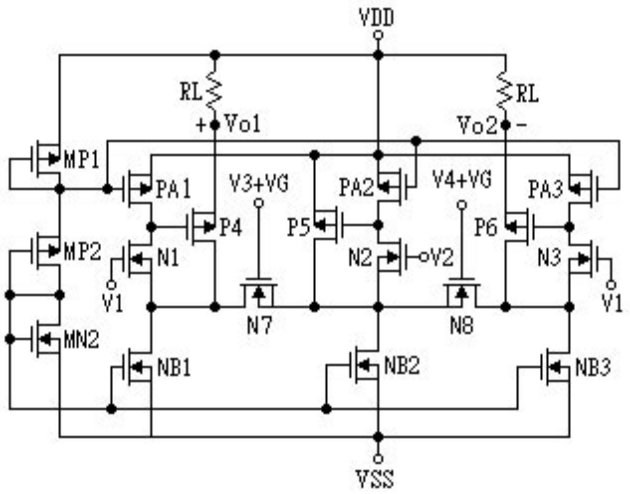

Fig. 1 The configuration of CMOS four-quadrant analogue multiplier.

Therefore a four-quadrant multiplier is obtained. The multiplication operation is performed by two differential variables ($V_3 - V_4$) and ($V_1 - V_2$). The voltage swing of the output can be determined by load resistor R_L. To ensure linear operation of the multiplier, the following constraints should be satisfied:

$$\max(V_1, V_2) < V_G + \sqrt{\frac{2I_{PA}}{K}} + V_{tn}(\text{N1}) - V_{tn} + \min(V_3, V_4)$$

Large signal nonidealities of the multiplier arise from many source and reflect themselves as nonlinearities and harmonic distortion. If the components are assumed to be matched, the main causes of nonlinearity are the channel length modulation and mobility reduction effects. The effect of channel length modulation can be greatly suppressed by using a regulated cascade (RGC) circuit. When deriving eqn.(1) to eqn.(6), the mobility reduction effect was neglected. In presence of this effect, eqn.(6) can be expressed in a Taylor series of the form.

$$I_D(\text{N7}) - I_D(\text{N8}) = a_1 V_{in} + a_3 V_{in}^3 + a_5 V_{in}^5 + \cdots\cdots \tag{8}$$

Clearly, the mobility reduction effect manifests itself as odd harmonics. The major contributor to the nonlinearity is a_3/a_1,

$$\frac{a_3}{a_1} = \frac{\theta^2}{4[1 + \theta\ (V_{CM} - V_{tn})]^2} \tag{9}$$

where θ is the mobility reduction coefficient and V_{CM} is the common mode input voltage. Eqn.(9) suggests that, as the common mode gate-source voltage decrease the distortion increases, which is the case for low voltage circuits. However, θ (V_{CM} − V_{tn}) is much smaller than unity, causing little increase in distortion.

III. Simulation Results

The circuit of Fig. 1 was simulated using HSPICE with parameters of Taiwan Semiconductor Manufacturing Corporation (TSMC) 0.8μm N-well CMOS process. Typical parameters are V_{tn} = 0.75V, V_{tp} = −0.9V; K_p = 32.71μA/V^2, K_n = 101.05μA/V^2; θ_n = 0.078V^{-1}, θ_p = 0.12V^{-1}. The width-to-length ratios for all transistors in Fig. 1 are listed in Table I. All simulations were performed with supply voltages of ±1.5V, R_L = 20kΩ, and with all NMOS transistors sharing the same bulk, connected to V_{SS}. Fig. 3 shows the DC transfer characteristics of multiplier circuit. Similar curves were obtained by interchanging ($V_1 - V_2$) and ($V_3 - V_4$). The circuit has less than 0.9% nonlinearity error over a ±0.8V differential input voltage range. The body effect of N7 and N8 causes the threshold voltage shift and introduces nonlinearity in the output current. For a 30kHz differential signal having a 0.8V peak amplitude applied to V_1 and V_2, with $V_3 - V_4$ held constant at 0.8V, the output voltage has a THD (Total Harmonic Distortion) less than 1%. An AC small signal frequency response of Fig. 4 shows a very flat response up to 15MHz. The simulation results are summarized in Table II.

Fig. 5 shows the amplitude modulation output waveforms with a 7mVp-p, 2.5kHz triangular signal applied to $V_3 - V_4$, 7mVp-p, 100kHz sinusoidal signal to $V_1 - V_2$.

TABLE I
ASPECT RATIOS OF MOS TRANSISTORS IN FIG. 1

MOS	PA1~PA3	NB1~NB3	N1~N3	P4~P6	N7,N8	MP1	MP2	MN2
W(μm) / L(μm)	5/15	30/5	25/5	50/5	2/20	10/30	350/2	6/10

TABLE II
SUMMARIZED SIMULATED RESULTS

Nonlinearity error ($\|V_1 - V_2\| \le 0.75$ V)	$\le$ 0.9%
Total harmonic distortions	$\le$ 1%
–3dB bandwidth	15MHz
DC dissipation power	24.4mW
Total input equivalent noise (30kHz)	9.1mV
Total output noise (30kHz)	0.2mV

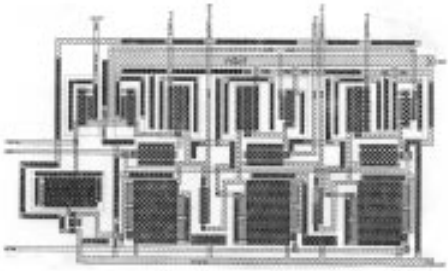

Fig. 2 Layout diagram of analogue four-quadrant multiplier.

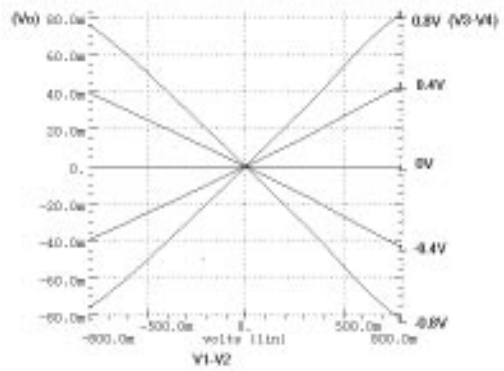

Fig. 3 Simulated DC transfer characteristics for R_L = 20kΩ.

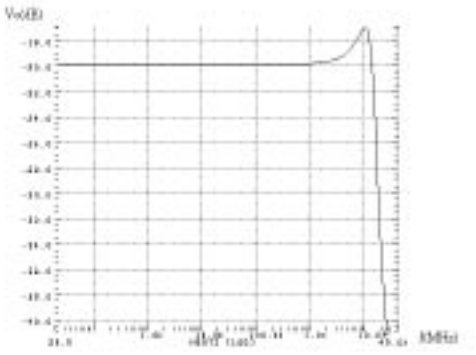

Fig. 4 –3dB frequency response of the multiplier.

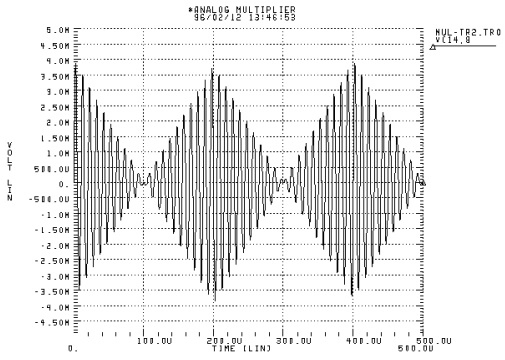

Fig. 5 2.5kHz triangular and 100kHz sinusoidal signal modulation.

IV. EXPERIMENTAL RESULTS

A test chip of the circuit in Fig. 1 was fabricated through CIC (Chip Implementation Center) in 0.8μm N-well CMOS technology. Two 15kΩ resistors as a loading was connected to the output of test chip. ±1.5V supplies and V_G = 1.1V were used. Fig. 6 shows the experimental V_{out} against $V_1 - V_2$ characteristics for constant values $V_3 - V_4$ = ±0.8V in 0.1V step. The linearity errors is less than 0.79% over a ±0.65V differential input range. Fig. 7 shows input and output waveform at –3dB frequency. Due to the loading effects from oscilloscope (1MΩ and 20pF) and parasitics from IC pads, –3dB frequency was shifted from 15MHz to 114kHz, which is close to the simulated results for considering instrumental loading (ω_{-3dB} = 121kHz).

The measured total harmonic distortion with 0.8V (peak) input signal at either input terminal with ±0.8V DC voltage at the other terminal is less than 2% for frequencies up to 30kHz.

Fig. 6 Measured DC transfer characteristics with $V_3 - V_4$ = ±0.8V for R_L = 15kΩ.

Fig. 8 shows the measured output waveforms with 0.4Vp-p 150kHz sinusoidal and 2.5kHz triangular input signals. A phase shift was noticed in the modulation process as compared with the lower triangular signal (negative amplitude) in Fig. 5, which was ascribed to be a nonzero DC offset of the

carrier signal (150kHz). A similar modulation waveform without the phase shift can be obtained if DC offset of the carrier signal is set to be zero. (not shown here due to limited space). A complete and detailed analysis for the results of above modulation signal processing will be further discussed in [12].

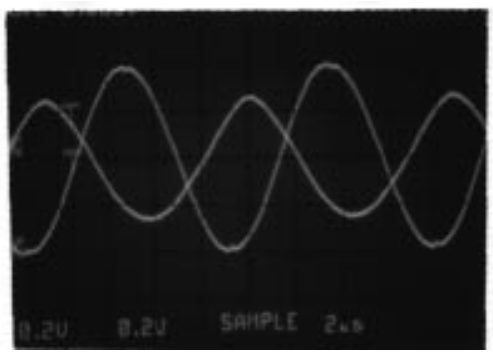

Fig. 7 Input and output waveforms at −3dB frequency.

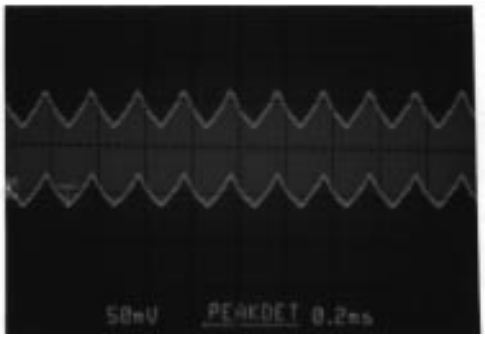

Fig. 8 Amplitude modulation output signal for 2.5kHz triangular and 150kHz sinusoidal input signals.

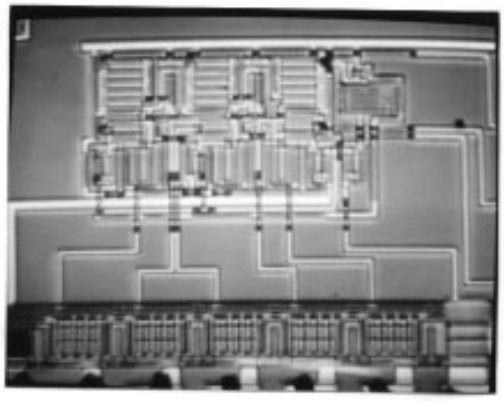

Fig. 9 Microphotograph of the test chip.

V. CONCLUSION

The multiplier reported in this paper operates from a ±1.5V supply voltages and has a linearity better than 0.8% for a differential input voltage range of ±650mV. This simple multiplier, using only two MOS transistors, operated in the triode region with modified bidirectional RGC structures to realize four-quadrant multiplication. Experimental and simulation results are given to demonstrate the feasibility of the proposed circuits. The operation principle of the multiplier is explained along with the examination of the second order effect. The proposed multiplier is more suitable for low voltage operation and expected to be useful in analog signal processing applications.

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