Optimal Loop Bandwidth Design for Low Noise PLL Applications

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Abstract— This paper presents a salient method to find an optimal bandwidth for low noise phase-locked loop (PLL) applications by analyzing a discrete-time model of charge-pump PLLs based on ring oscillator VCOs. The analysis shows that the timing jitter of the PLL system depends on the jitter in the ring oscillator and an accumulation factor which is inversely proportional to the bandwidth of the PLL. Further analysis shows that the timing jitter of the PLL system, however, proportionally depends on the bandwidth of the PLL when an external jitter source is applied. The analysis of the PLL timing jitter of both cases gives the clue to the optimal bandwidth design for low noise PLL applications. Simulation results using a C-language PLL model are compared with the theoretical predictions and show good agreement.

I. Introduction

In modern data transmission systems such as local area networks, disk drive system, telecommunication networks, and optical communication systems, information is transmitted or received in the form of either baseband or passband signals containing sequences of digital symbols. In these applications, usually only data signals are transmitted by the transmitter and separate clock signals used to synchronize the data are not transmitted to save the expense of the interconnection and hardware. Therefore, the receiver should extract the clock information from the received data using a circuit block, called the clock recovery circuit, and synchronize the data with the extracted clock. Most of the clock recovery circuits contain at least a PLL due to its excellent performance in extracting the clock information[1][2].

In clock synthesis systems such as video, audio, and data processors, several sets of clocks are usually required to meet the different frequency requirements for the internal signals. In these applications, those multiple frequencies for the clocks should be generated from an external reference clock which has a fixed frequency. In this case, the clock synthesis system uses a circuit block, called the frequency multiplication circuits based on a PLL with frequency dividers[3][4].

As clock rates go higher, more stringent requirements are put on the PLLs toward reducing the PLL noise because it increases error rates of a system. In the clock recovery system, the VCO(voltage controlled oscillator) in the PLL is locked to the incoming noisy data bit stream and the PLL is required to reduce the noise in order to generate low noise output clock. However, in the clock synthesis system, the VCO is locked to a low noise reference, often in the form of crystal. In this system, the output noise is mainly affected by the internal noise sources such as the VCO, phase detector etc. In both cases, it will be shown that there is a trade-off involved in selecting the bandwidth of the PLL. A narrow bandwidth PLL rejects input noise very well but does not correct the VCO timing errors as quickly, leaving the total output noise unreduced. On the other hand, a wide bandwidth PLL can correct VCO errors more quickly but if made too wide, leaves the system input noise unreduced.

Because the noise environments of both system are different, the bandwidth requirements are also different. The goal of this paper is to estimate the root mean square (rms) phase noise (jitter) of a PLL clock output and find the optimum bandwidth which gives the best noise performance for each system. In section II, the noise analysis is performed to obtain the total output jitter and the equation for the optimum bandwidth is derived from the analysis. Section III presents some design examples and simulations with a behavioral model of a charge-pump based PLL. Finally, in section IV, conclusions are drawn.

II. PLL Optimal Loop Bandwidth

The basic jitter analysis for a given internal VCO jitter source has been published in [5]. However, to create the logic connection to the overall analysis some material here are repeated in this paper. As mentioned in [5], the timing jitter in a ring-oscillator PLL depends on the interaction of noise in the oscillator with the dynamics of the phase-locked loop. It has been shown in [5] that the

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timing jitter variance at the end of a chain of inverters is given by the sum of the contributions of each stage. If each stage contributes a timing error with variance $\delta\tau_n^2$, then the total jitter at the end of N stages is $N\delta\tau_n^2$. In a ring-oscillator this timing error determines the starting point of the next cycle and therefore creates a permanent phase shift in the output signal. If the ring-oscillator is configured in a phase-locked-loop, however, the phase difference between the reference clock and the oscillator output is detected and compensated by the dynamics of the loop. The phase detector will sense the shift and create an error signal to change the frequency of the ring-oscillator VCO in a way which moves the phase of the output in the right direction.

Since the amount of phase adjustment is usually small, the phase error is not corrected in one clock cycle, but it is reduced gradually over the course of several cycles. The phase error may remain for up to several hundreds of cycles, depending on the bandwidth of the loop filter in the PLL.

Analysis of the accumulated phase jitter and its relation to the loop bandwidth is important for both clock synthesis and clock recovery applications. In most PLL clock synthesizer designs, the reference clock comes from a very low jitter source such as crystal oscillator. Therefore, the jitter in the ring-oscillator is the main source of the phase error in the synthesized clock. For clock recovery applications there is a trade-off involved in the choice of the loop bandwidth since the input signal that is being locked to is not ideal, but has timing jitter associated with it as well. A narrow loop-band width will reduce the impact of jitter in the input signal since the loop will not try to track input fluctuations as strongly. On the other hand, this means that it will take more time to compensate for the jitter events in the ring-oscillator. Previously, more attention has been paid to the first effect than the second, but both are important for high performance clock recovery applications. So for both clock synthesis and clock recovery applications, a thorough analysis of the output jitter due to the internal jitter sources as well as the external jitter source is important [6].

To find the accumulated rms jitter, a PLL which uses a sequential phase detector and a charge-pumping circuit (Fig.1) is represented by a simple discrete-time model as shown in (Fig.2)[7]. The transfer function for jitter in the PLL due to the internal jitter sources is represented by (1) in z-transform domain.

$$\Theta_{on}(z) = \frac{\Theta_{ni}(z)}{1 + K_d K_v Z_F(z) z^{-1}} \tag{1}$$

Here the phase detector gain and VCO gain is given by $K_d = \frac{I_s}{2\pi}$ and $K_v = \frac{dw}{dv}$ respectively. I_s indicates charge pumping current and the $Z_F(z)$ represent the Z transform of $\frac{H(s)}{s}$, where H(s) is the transfer function of the PLL loop filter(Fig.3).

$$H(s) = \frac{1}{sC_2} \| (\frac{1}{sC_1} + R) \cong R\frac{1}{s}(s + \frac{1}{RC_1}) = a \cdot \frac{1}{s}(s + b) \tag{2}$$

Here the loop filter impedance $H(s)$ can be reduced to first order if the ratio of $\frac{C_2}{C_1}$ is less than 1. In this case, a represent the gain of the loop filter, and b represent the zero of the filter. Then,

$$\begin{aligned} Z_F(z) &= T \cdot Z\left(L^{-1}\left[\frac{H(s)}{s}\right]_{t=nT}\right) \\ &= aT \cdot \frac{z^2 + (bT-1)z}{(z-1)^2} \cong aT \cdot \frac{z}{z-1} \end{aligned} \tag{3}$$

Since the PLL input data rate, $\frac{1}{T}$, is larger than the zero b of the filter, the product, bT in equation (3), is negligible. Therefore, the (1) can be rewritten as (4).

$$\Theta_{on}(z) = \frac{1 - z^{-1}}{1 - (1-\epsilon)z^{-1}}\Theta_{ni}(z) \quad , where\ \epsilon = K_d K_v aT \tag{4}$$

In the equation (4) the timing jitter $\Theta_{ni}(z)$ from the ring oscillator can be modeled as a sequence of unit step phase jump with random magnitude. And a single phase jump at time nT can be represented by (5).

$$\Theta_{ni}(z) = \frac{2\pi\delta\tau_r}{T}\frac{1}{1 - z^{-1}} \tag{5}$$

where $\delta\tau_r$ is the magnitude of the error step in the vco phase. Then the output jitter at time nT in equation (4) can be rewritten as (6) in z domain.

$$\Theta_{on}(z) = \frac{2\pi\delta\tau_r}{T}\frac{1}{1 - (1-\epsilon)z^{-1}} \tag{6}$$

To see the result of the phase error in the time domain, equation (6) needs to be transformed to time domain.

$$\Theta_{on}(nT) = \frac{2\pi\delta\tau_r}{T}(1-\epsilon)^n u(nT) \tag{7}$$

The summation of output timing error is represented by (8).

$$\Theta_{tot}(nT) = \sum_{k=-\infty}^{n}\left(\frac{2\pi\delta\tau_k}{T}(1-\epsilon)^{n-k}\right) \tag{8}$$

To find out the r.m.s. output jitter, the expectation of the square of the sum(8) is calculated and represented by (10). Where the r.m.s. of the ring oscillator $\delta\tau_r$, $\delta\tau_l$ are not correlated with different time sample. As a result, $E[\delta\tau_r\delta\tau_l]$ is 0, when $r \neq l$ and $\delta\tau_r^2$, when $r = l$.

$$\begin{aligned} E[\Theta_{tot}^2(nT)] &= \left(\frac{2\pi}{T}\right)^2 \delta\tau_r^2 \sum_{k=-\infty}^{n}(1-\epsilon)^{2(n-k)} \\ &= \left(\frac{2\pi}{T}\right)^2 \delta\tau_r^2 \frac{1}{\epsilon(2-\epsilon)} \\ &= \left(\frac{2\pi}{T}\right)^2 \frac{\delta\tau_r^2}{2\epsilon} \quad , where\ \epsilon \ll 1 \end{aligned} \tag{9}$$

$$\sqrt{E[\Theta_{tot}^2(nT)]} = \sqrt{\frac{1}{2\epsilon}}\left(\frac{2\pi}{T}\right)\delta\tau_{1rms} \qquad (10)$$

where $\delta\tau_{1rms} = \sqrt{\delta\tau^2}$, and the product K_dK_vR is selected less than $\frac{1}{T}$. According to the equation (10), total rms output jitter due to internal VCO phase is inversely proportional to the loop bandwidth of the PLL. Consequently, increasing the PLL loop bandwidth decreases the jitter accumulation in the output under the condition of $bT \ll 1$, $\epsilon \ll 1$.

To find the output jitter caused by the external jitter source, the same model is used except that the jitter source moved from the VCO to the input. Then, the transfer function for the PLL output jitter due to the input jitter source is represented by (11) in the z-transform domain.

$$\Theta_{orn}(z) = \frac{K_dK_vZ_F(z)z^{-1}}{1+K_dK_vZ_F(z)z^{-1}}\Theta_{nr}(z) \qquad (11)$$

In the equation (11) the timing error input $\Theta_{nr}(z)$ from the external input jitter source can be modeled as a sequence of single pulse with random magnitude. And a single phase pulse at time nT can be represented by (12).

$$\Theta_{nr}(z) = \frac{2\pi}{T}\delta\tau_s \qquad (12)$$

where $\delta\tau_s$ is the magnitude of the error pulse. Then the output jitter at time nT can be rewritten as (13) using the equation (3) and (12).

$$\Theta_{orn}(z) = \frac{2\pi\delta\tau_s}{T}\frac{\epsilon z^{-1}}{1-(1-\epsilon)z^{-1}} \quad , where\ \epsilon = K_dK_vaT \qquad (13)$$

Then jitter output in the time domain is shown (14) by inverse-z-transform.

$$\Theta_{orn}(nT) = \frac{2\pi\delta\tau_s}{T}\epsilon\cdot(1-\epsilon)^{n-1}u[(n-1)T] \qquad (14)$$

The summation of output timing error is represented by (15).

$$\Theta_{tot}(nT) = \sum_{k=-\infty}^{n}\left(\frac{2\pi\delta t_k}{T}\cdot\epsilon(1-\epsilon)^{n-k+1}\right) \qquad (15)$$

To find out the r.m.s. output jitter due to the external input jitter sources, the expectation of the square of the sum (15) is calculated and represented by (16). Where the r.m.s. of the external input jitter $\delta\tau_s$,$\delta\tau_l$ are not correlated with different time samples.

$$\begin{aligned}\sqrt{E[\Theta_{tot}^2(nT)]} &= \sqrt{\frac{\epsilon}{2}}(1-\epsilon)\left(\frac{2\pi}{T}\right)\delta\tau_{2rms} \\ &\cong \sqrt{\frac{\epsilon}{2}}\left(\frac{2\pi}{T}\right)\delta\tau_{2rms} \qquad (16)\end{aligned}$$

where $\delta\tau_{2rms} = \sqrt{\delta\tau^2}$, and the product K_dK_vR is selected less than $\frac{1}{T}$. By combining equation (10) with (16), we can get the total PLL output rms jitter(17).

$$\begin{aligned}\sqrt{E[\Theta_{tot}^2(nT)]} &= \sqrt{\frac{1}{2w_nT}}\left(\frac{2\pi}{T}\right)\delta\tau_{1rms} + \\ &\sqrt{\frac{w_nT}{2}}\left(\frac{2\pi}{T}\right)\delta\tau_{2rms} \qquad (17)\end{aligned}$$

It is found that the output rms jitter is inversely proportional to the $\epsilon = K_dK_vaT$ when the internal jitter is applied and proportional to when the external input jitter source is applied. Here, the parameter ϵ is represented by the product of the loop bandwidth parameter $w_n = K_dK_va$ and the data rate T.

Minimization of equation (17) gives us the optimal PLL bandwidth W_{opt}.

$$W_{opt} = \frac{1}{T}\left(\frac{\delta\tau_{1rms}}{\delta\tau_{2rms}}\right) \qquad (18)$$

where the $\delta\tau_{1rms}$ is the r.m.s jitter of the internal vco phase, $\delta\tau_{2rms}$ is the r.m.s. jitter of the external input reference, and the T is the clock period of the PLL. According to the equation (18), the optimal loop bandwidth of the PLL is closely related with the rms jitter of the input source and the internal VCO and the clock period of PLL.

III. Design example and Simulation

To verify the analysis, the PLL is modeled by C-language with the configuration shown in Fig.4. The simulator uses the white gaussian random number generation for the jitter process including the effect of the noisy delay cells in the VCO and the nonlinear physical channel effect and environmental noise in the input.

The parameter of the PLL should be chosen carefully for fast locking and stable operation. The parameter can be decided from the viewpoint of the second order system such as damping factor and natural frequency of the PLL although the third order PLL is used. There is no clear-cut design process, however, for the third order PLL because of the complexity in controlling the system parameter. If the capacitor of the loop filter, C_2, be made less the 20 times the C_1, the second order model is enough.

Simulation result of the timing jitter output with varying was shown in Fig.5, and indicates that there is the optimum bandwidth which minimizes the PLL output jitter. The obtained bandwidth from the simulation result agrees with their analysis. The VCO internal rms jitter is usually very small ($\sim$ ps), but the input rms jitter varies a lot with the applications. Therefore in the timing recovery system, where the input jitter dominates, the narrow bandwidth should be chosen as shown in Fig.5(lower). However, in the case of clock synthesis system, there is concave function which has the optimum point generating low noise as shown in Fig.5(upper). Fig.6 shows the analytical simulation of the output jitter with the same

parameter T_d=internal jitter, T_i=external input jitter of the above behavioral simulation. This makes a close resemblance between them. The optimal bandwidth of the PLL in the above simulation is about 400KHz in the low jitter input case and about 4KHz in the large amount of input jitter.

Here, the decision of the optimal bandwidth requires the parameters such as, the reference jitter variance, the internal VCO variance and the system clock periods.

IV. Conclusion

In this paper, the estimation of the root mean square phase noise of a PLL output taking external and internal noise source are presented with the behavioral PLL model simulations verifying the analysis. In the various noise environment requiring various loop bandwidth, the design of optimal bandwidth with good noise performance, can be made through the analytic phase noise model, taking physical parameters such as external noise variance, internal noise variance and system periods.

Simulation results using a charge-pump PLL model shows good agreement with the theoretical predictions. This analysis can be used both in clock recovery and in clock synthesis which requires good noise performance in the PLL.

References

[1] B.Kim, J.D.Greco, H.C.Yang, W.S. Wu, and R.F.Chowdhury, "An integrated CMOS mixed-mode signal processor for disk driv e read channel applications", *IEEE Trans. Circuits Syst.*, Vol.CAS-41, no.1, pp. 1-18, Jan. 1994.

[2] R. Saban and A. Efendovich, "A fully-digital, 2-MB/sec, CMOS data separator", *Proc. 1994 Int. Symp. Circuits Syst.(London)* , Vol. 3, pp. 53-56, June 1994.

[3] Reza Shariatdoust, K. Nagaraj, Martin Saniski, and Joseph Plany, "A Low Jitter 5MHz to 180MHz Clock Synthesizer for Video Graphics", *IEEE Custom Integrated Circuits conference*,

[4] Loke K.Tan, Edward Roth, Gordon E. Yee, Henry Samueli, "An 800MHz Quadrature Digital Synthesizer with ECL-Compatible Output Drivers in 0.8um CMOS", *ISSCC Digest of Technical Papers*, , pp258-259, Feb, 1995.

[5] Todd C.Weigandt, Beomsup Kim, Paul R.Gray, "Timing Jitter Analysis for High-Frequency, Low-Power Oscillator Design", *ISCAS* , June 1994

[6] Beomsup Kim, "High Speed Clock Recovery in VLSI Using Hybrid Analog/Digital Techniques" *UCB/ERL Memorandum*, June 1994.

[7] Floyd M. Gardner, "Charge-Pump Phase-Locked Loops", *IEEE Trans on Communications*, vol.COM-28, no.11, Nov, 1980.

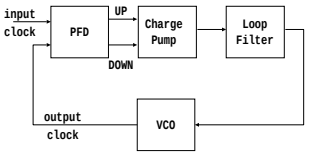

Fig. 1. Charge Pump Phase-Locked Loop

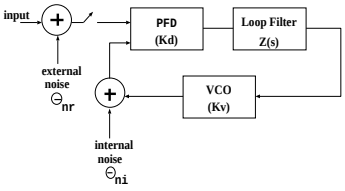

Fig. 2. Simplified PLL Discrete Time Model

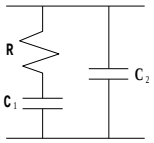

Fig. 3. Loop filter Structure

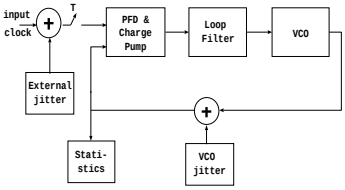

Fig. 4. Discrete time PLL with simulation setup

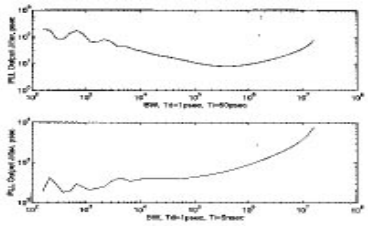

Fig. 5. Jitter accumulation with Behavioral model (upper Clock synthesis app.) (lower Clock Recovery app.)

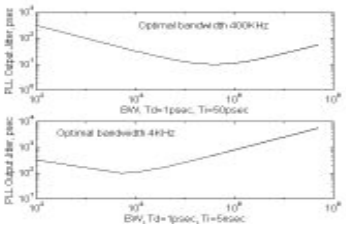

Fig. 6. Jitter accumulation with Analytic model