Analysis and Design of Multiple-Bit High-Order Σ-Δ Modulator

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Abstract— **The high-order Σ-Δ modulator is an appropriate approach for high-bandwidth, high-resolution *A/D* conversion. However, non-ideal effects such as the finite op-amp gain and the capacitor mismatch have great impacts on its performance at a low oversampling ratio. To achieve greater performance under the inevitable non-ideal effects, we explore several multiple-bit schemes, based on our CIQE high-order Σ-Δ architecture, to remove the non-ideal deterioration. Design rules of these multiple-bit schemes are developed and verified by extensive simulations.**

I. Introduction

The A/D converter is an important element for digital-signal processing systems. The cruxes of an A/D converter are high resolution for precise representation of the original signal and high bandwidth for fast processing. Conventional A/D architectures, e.g., flash, 2-step flash, and successive approximation, are not suitable for high-resolution applications because of the need of near-ideal analog components and/or precise trimming. To implement a high-resolution A/D converter, the Sigma-Delta modulator (SDM) is considered a suitable approach and widely used due to its simplicity and effectiveness [1].

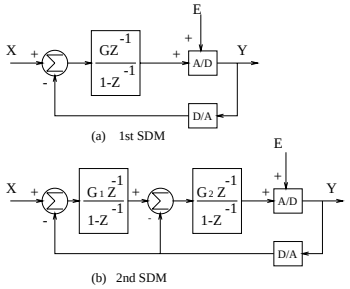

Fig. 1. (a) First-order SDM. (b) Second-order SDM.

Fig. 1 depicts two popular SDMs: the first-order and the second-order ones. Though able to achieve high resolution, the SDMs must operate under a sufficiently high over-sampling ratio, which in turn limits the input bandwidth [1–4]. For applications requiring both a high resolution and a high bandwidth, a high order SDM should be used instead [5].

The hypothetical N-th order SDM has the following I/O relationship:

$$Z_{x_A}(z)\,X(z) + (1-z^{-1})^N E(z) = Y_A(z), \qquad (1)$$

where $Z_{x_A}(z)$ represents the possible modification of the input signal $X(z)$. Generally, $Z_{x_A}(z)$ exhibits an ideal all-pass frequency response in the signal band (baseband) with a possible linear-phase delay so as to pass the signal without skew, except for a pure delay and attenuation. Note that $(1-z^{-1})^N$ is a baseband noise-depressing filter which attenuates the noises out to the high-band. Consequently, the output $Y_A(z)$ resembles the input $X(z)$ in baseband with a slight deterioration exclusively caused by the baseband-depressed noise source $E(z)$. The larger N is, the less $E(z)$ affects the final output. Thus, A high signal-to-noise ratio (SNR) can be obtained if N can be made larger. Several works on high-order SDMs have been published [6–11].

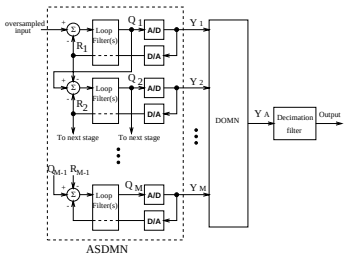

Fig. 2. The M-stage N-th order CIQE SDM architecture.

In [5], a general high-order SDM architecture—the *cascaded intermediate quantization error* (CIQE) architecture—is proposed and shown to be a better approach for high-order SDM applications. It consists of three functional blocks: the analog SDM network (ASDMN) for oversampling the external analog signal, the digital output mixture network (DOMN) for mixing the intermediate quantized signals, and the decimation filter to remove high-band noise from the final digital output [12]. The M-stage N-th order CIQE SDM has the profile as shown in Fig. 2. In practical applications, each of the M SDM stages in Fig. 2 is of order n_i, $1 \le n_i \le 2$, $1 \le i \le M$, such that $\sum_{i=1}^{M} n_i = N$. DOMN is a multiple-input single-output system having the following transfer function:

$$Y_A(z) = \sum_{l=1}^{N-1} \left(\prod_{k=1}^{N-l} Z_{x_{N-k+1}}(z) \right) (1-z^{-1})^{\sum_{i=1}^{l-1} m_i} Z_{y_l}(z) Y_l(z) + (1-z^{-1})^{\sum_{i=1}^{N-1} m_i} Z_{y_N}(z) Y_N(z). \qquad (2)$$

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In Fig. 2, $E_i = Q_i - R_i$, $1 \le l < M$, are the *intermediate quantization errors* at the corresponding stages, while E_M is the *intrinsic quantization error*. Each E_i, represents the quantization error of the A/D-D/A loop in the corresponding stage, and can be considered as an *additive white Gaussian noise* (AWGN) with a power spectral density of $\frac{\Delta^2}{12}$ [13]. Analysis has been made to explore the characteristics of different ASDMN organizations, and simulation results show that a total signal-to-noise ratio (TSNR) of 102dB under an oversampling ratio of as low as 16 can be achieved by using a 7-th order CAFO SDM (a CIQE-based SDM made up of only first order SDMs in its ASDMN) [5]. In the context, TSNR is defined as the ratio of the signal power to the total power of the noises and harmonic distortions.

In spite that CIQE configuration behaves well under ideal-case simulations, non-ideal effects such as finite op-amp gain and capacitor mismatch have great impacts on its performance when the oversampling ratio is very low [14–16]. Hence, higher quality components are required for high-order CIQE SDM to achieve the high-resolution capability. In this paper, to preserve the performance of high-order SDMs under the non-ideal circuit effects, we propose several multiple-bit schemes to reduce performance deterioration caused by the non-ideal effects. The multiple-bit schemes remove the requirement of high-quality circuits in previous CIQE SDM designs [16], and help providing higher TSNR for the conventional low-order and high oversampling-ratio SDM. We first give quantitative analysis to explore the relationship between the non-ideal effects and the noises induced. Multiple-bit schemes are then introduced to remove the noises and some implementation specifications are presented. Simulations are also made to validate our multiple-bit solutions.

II. Sources of Errors

So far the CAFO SDM is the most cost-effective design for high-bandwidth, high-resolution applications. However, it is shown that non-ideal effects will deteriorate the CAFO SDM [16]. We now demonstrate how the non-ideal effects influence the CAFO SDM. Other CIQE-based SDMs can be analyzed in a similar way [16].

In the CIQE architecture, non-ideal effects are attributed to the analog block, including the loop filter and the quantizer at each stage of the SDM in the ASDMN. The loop filter is generally an integrator. Non-ideal effects such as the finite op-amp gain and the capacitor mismatch deteriorate the loop filter of an SDM to be $\frac{\alpha z^{-1}}{1-\beta z^{-1}}$ rather than $\frac{z^{-1}}{1-z^{-1}}$ in the ideal circuit, where α and β represent the non-ideal gain and the non-ideal integration factor of the integrator, respectively.

Consider the non-ideal loop filters in our high-order CAFO SDM. Substituting $\frac{Gz^{-1}}{1-z^{-1}}$ with $\frac{\alpha z^{-1}}{1-\beta z^{-1}}$ in $Y_A(z)$ yields

$$Y_A(z) = \frac{\alpha z^{-M} X(z)}{1+(\alpha-\beta)z^{-1}} + \sum_{l=1}^{M-1} Z_{E_l}(z)E_l(z) + Z_{E_M}(z)E_M(z), \quad (3)$$

where

$$Z_{E_l}(z) = \frac{(1-\alpha+(\alpha-\beta)z^{-1})}{1+(\alpha-\beta)z^{-1}} z^{-(M-l)}(1-z^{-1})^{l-1} \quad (4)$$

for $1 \le l < M$ and

$$Z_{E_M}(z) = \frac{1}{(1+(\alpha-\beta)z^{-1})} \cdot \frac{1-\beta z^{-1}}{(1-z^{-1})}(1-z^{-1})^M. \quad (5)$$

In [16] it is shown that $\frac{\alpha z^{-M}}{1+(\alpha-\beta)z^{-1}}$ is a constant with a value close to 1 in baseband, i.e., the CAFO SDM will pass the input signal $X(z)$ to the combined digital output $Y_A(z)$ without distortion, except for a little attenuation. Thus, in the baseband, we have

$$Y_A(z) = X(z) + Z_{E_M}(z)E_M(z) + \sum_{l=1}^{M-1} Z_{E_l}(z)E_l(z). \quad (6)$$

The intermediate errors E_i, $1 \le i < M$, do not vanish as in the ideal case because of the non-ideal α and β, and they are defined as the *leakage errors*. Eq. (6) illustrates that $Y_A(z)$ is additionally contaminated by the leakage errors $E_i(z)$, $1 \le i < M$, besides the intrinsic quantization error noise $E_M(z)$.

Let f_s be the sampling frequency and R the oversampling ratio, and $\xi^t_{E_i}$ denote the noise power caused by leakage error $E_i(z)$. Then, we have

$$\xi^t_{E_i} = \frac{\Delta_i^2}{24\pi} \int_0^{2\pi f_b} \left| \frac{(1-\alpha+(\alpha-\beta)e^{-j\omega T})}{1+(\alpha-\beta)e^{-j\omega T}} (1-e^{-j\omega T})^{i-1} \right|^2 d\omega, \quad (7)$$

where $f_b = \frac{f_s}{R}$ is the bandwidth of the oversampled input signal. Note that $(1-e^{-j\omega T})^{i-1}$ is a baseband-depressing filter, so the effect of the leakage error of a later stage is less than that of its preceding stage if all coarse quantizers in ASDMN have the same resolution. Generally, we have

$$\xi^t_{E_{M-1}} < \xi^t_{E_{M-2}} < \ldots < \xi^t_{E_2} < \xi^t_{E_1}. \quad (8)$$

The noise power of the leakage errors is far more than that of the intrinsic quantization error unless near-ideal circuits are available [16]. The leakage error E_1 has more noise power impact than the others. It is the dominant leakage error in our multiple-bit schemes.

III. Multiple-Bit Schemes

The non-ideal effects depend not only on the circuits we use to implement the CAFO SDM but also on the oversampling ratio. The stray-insensitive integrator depicted in Fig. 3 is a popular choice for SDM implementation. We will use it as the loop filter of our SDMs for examples. We assume the oversampling ratio is 16 to analyze the benefits of the multiple-bit schemes quantitatively. The non-ideal factors of α and β of the stray-insensitive integrator can be found to be $\alpha = \frac{G}{1+\mu(1+G)}$ and $\beta = \frac{1+\mu}{1+\mu(1+G)}$ where $G = \frac{C_2}{C_1}$ and μ is the reciprocal of the op-amp gain.

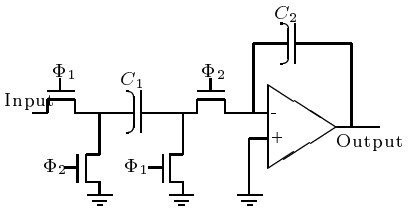


Fig. 3. Single-ended version of the stray-insensitive integrator.

A. Simple Multiple-Bit (SMB) Scheme

If near-ideal analog circuits are available, then the non-ideal effects which result in the leakage errors in (6) can be neglected, and the I/O relationship of the N-th order CIQE SDM becomes (1). The only noise component of Y_A in the CAFO SDM is the intrinsic quantization error term $(1-z^{-1})^N E_M$. To reduce the noise effect of this error, a multiple-bit technique can be applied to the last SDM stage in ASDMN. The total noise power, denoted by ξ_t, can be expressed as

$$\xi_t = \frac{1}{2\pi}\int_0^{2\pi f_b} |(1-e^{-j\omega T})^M E_M|^2 d\omega = \Delta^2 F(M, f_b), \tag{9}$$

where Δ is the quantization step of the last SDM stage. Eq. (9) shows that the effect of the intrinsic error can be alleviated by refining the quantization step with a smaller value of Δ, i.e., by using multiple-bit representation of the quantized output at the final stage. This is called the simple multiple-bit (SMB) scheme. To be more specific, with one more bit used, ξ_t is successively reduced to a quarter of the original value. We have

$$\xi_t^n = (\frac{1}{4})^{n-1}\xi_t,\ n \geq 1, \tag{10}$$

where ξ_t^n is the noise power with n-bit SMB scheme.

The SMB scheme is direct and simple but has only limited applications due to the fact that the intrinsic quantization error is usually far less than the leakage errors in high-order (and/or low oversampling ratio) SDM applications. In practice, the near-ideal circuits are available only if the SDM has a low order and operates under a high oversampling ratio. The reason is that the leakage error should be made less than the intrinsic quantization error to make the circuits near-ideal. The leakage error power of a CAFO SDM will later be shown (see (12)) to be proportional to the reciprocal of the product of the oversampling ratio and the square of the op-amp gain. Consequently, this SMB scheme is valid only if we have a high oversampling ratio and/or the circuit components are near-ideal. Related discussions of this SMB scheme can be found in [17].

B. Full Stage Multiple-Bit (FSMB) Scheme

According to (6) and (7), the noise sources of the quantized output of the CAFO SDM are the leakage errors and the intrinsic quantization error. They are all proportional to the square of the quantization step Δ. A straightforward method to alleviate the noises is then making Δ smaller while keeping the signal power unchanged. This can be done by replacing all the single-bit quantizers with multiple-bit quantizers. The noise sources will have a power spectral density of $\frac{1}{12}\left(\frac{\Delta}{2^n}\right)^2$ if n-bit quantizers are used. Consequently, the noise power ξ_t^n of the n-bit FSMB SDM becomes

$$\xi_t^n = (\frac{1}{4})^{n-1}\xi_t^1,\ n \geq 1, \tag{11}$$

where ξ_t^1 is the total noise power of the conventional CAFO SDM with all-single-bit (ASB) quantizers. Eq. (11) indicates that increasing n will decrease the total noise power. This method is referred to as the full stage multiple-bit (FSMB) scheme.

FSMB is not a cost-effective scheme due to the excessive hardware complexity. For example, if we want 2 more bits (12dB) for a 7-th order CAFO SDM, we need 55 additional comparators and D/A capacitors. By (6), there are two noise sources. Usually, the leakage error dominates the others under the non-ideal situation [16]. This property implies that the multiple-bit schemes can be done effectively by applying multiple-bit quantizers only to the dominant noise source, which is shown next.

C. Single-Stage Multiple-Bit (SSMB) Scheme

Eq. (8) reveals that the noise power of the leakage error from the first SDM stage, ξ_{E_1}, dominates the total noise power. Consider a practical application where the stray-insensitive integrators are used as the loop filters. The noise power consists of the following.

1. Noise power due to the finite op-amp gain, $\xi_{E_1}^{fg}$. The op-amp gain (μ^{-1}) is a finite value while assuming all other components are ideal. It can be shown [16] that

$$\xi_{E_1}^{fg} = \frac{\Delta^2\mu^2}{12(1+2\mu)^2}(\frac{5}{R} - \frac{2}{\pi}\sin(\frac{2\pi}{R})). \tag{12}$$

2. Noise power due to the capacitor mismatch, ξ_{E1}^{cv}. Given the op-amp with a finite gain, the mismatch of the capacitors results in nonzero $|\triangle G|$ to the nominal value G. The corresponding noise power is [16]:

$$\xi_{E_1}^{cv} = \frac{\Delta^2\mu|\Delta G|}{12}\left|\frac{-6}{R(1+2\mu)^2} + \frac{3}{\pi(1+2\mu)^2}\sin(\frac{2\pi}{R})\right|. \tag{13}$$

ξ_{E1}^{cv} is generally not as important as ξ_{E1}^{fg}, since the capacitor-mismatch can be made as small as 0.1% by using a larger unit capacitor [16], though doing so has the disadvantages of a large area cost as well as a possible degradation of the sampling frequency. Consequently, the leakage power in the light of capacitor-mismatch can be alleviated easily if the area cost is the second consideration. Note that in a traditional design of low-order SDM, the oversampling ratio R can not be made small for high-resolution consideration; thus, ξ_{E1}^{cv} is negligible since $\sin(\frac{2\pi}{R}) \approx \frac{2\pi}{R}$ in conventional SDMs. It is not the case in our CAFO

SDM because it can provide a TSNR of 102dB under an oversampling ratio as small as 16. Instead, we use a large unit capacitor to alleviate this leakage power.

3. Apart from the integrators, the rest of ASDMN are the quantizers. There are several non-ideal effects in the quantizers which result in more noise power; however, they are negligible compared with ξ_{E1}^{fg} and ξ_{E1}^{cv} [16].

As a result, the noise power coming from the 1st SDM stage, $\xi_{E_1}^t$, under non-ideal considerations can be written as $\xi_{E1}^t = \xi_{E_1}^{fg} + \xi_{E_1}^{cv} \approx \xi_{E_1}^{fg}$. The noise power of the other intermediate quantization errors E_i^t, $2 \le i \le M$, can be derived in a similar way. The total noise power is

$$\xi_t = \sum_{i=1}^{M} \xi_{E_i}^t \approx \sum_{i=1}^{M} \xi_{E_i}^{fg}. \tag{14}$$

Let Δ_1 and Δ_2 be the quantization steps of the first two SDM stages in ASDMN. We have

$$\xi_{E_2}^{fg} == \frac{\Delta_2^2 \mu^2}{12(1+2\mu)^2}\left(\frac{14}{R} - \frac{9}{\pi}\sin\left(\frac{2\pi}{R}\right) + \frac{1}{\pi}\sin\left(\frac{4\pi}{R}\right)\right) \tag{15}$$

for our CAFO SDM. Substituting $R = 16$ into (12) and (15), we obtain

$$\begin{cases} \xi_{E_1}^t = 0.0689\Delta_1^2; \\ \xi_{E_2}^t = 0.0038\Delta_2^2. \end{cases} \tag{16}$$

If $\Delta_1 = \Delta_2$, then ξ_{E_2} is about 6% of ξ_{E_1}. Similar results can be found between ξ_{E_i} and $\xi_{E_{i+1}}$ for $2 \le i < M$. Therefore, the relationship of (8) can be expressed more precisely as

$$\xi_{E_M}^t << \xi_{E_{M-1}}^t << \ldots << \xi_{E_2}^t << \xi_{E_1}^t. \tag{17}$$

E_1 is then referred to as the dominant leakage error with the dominant noise power $\xi_{E_1}^t$. Since E_1 is the dominant leakage error, our single-stage multiple-bit (SSMB) scheme has a multiple-bit quantizer exclusively in the first SDM stage.

Let the first SDM stage has an n-bit quantizer. With the SSMB scheme, the SNR of the CAFO SDM can be expressed as

$$\begin{aligned} SNR &\equiv \frac{\xi_{signal}}{\xi_{noise}} \approx \frac{\xi_{signal}}{\xi_t} \approx 10log(\frac{\frac{\Delta^2}{8}}{\xi_{E_1}^t}) \\ &\simeq -10\log\left[\frac{\Delta_1^2}{\Delta^2}\left(\frac{2\mu^2}{3}\left(\frac{5}{R} - \frac{2}{\pi}\sin\left(\frac{2\pi}{R}\right)\right)\right)\right] \\ &= 6.02\,(n-1) - 10\log\left[\frac{2\mu^2}{3}\left(\frac{5}{R} - \frac{2}{\pi}\sin\left(\frac{2\pi}{R}\right)\right)\right] \end{aligned} \tag{18}$$

Eq. (18) reveals that increasing one bit of resolution for the intermediate quantized output at the first SDM stage will eventually result in one extra bit of resolution (6dB) at the final decimated output. Though it seems that the increased resolution is proportional to that in the quantizer at the dominant SDM stage, it should be noted that the resolution of the quantizer is larger than 3 when $R = 16$. Recall that (18) is valid only when (17) is true. Let n_1 and n_2 be the resolution in number of bits for the intermediate quantized outputs in the first and the second SDM stages, respectively. Since the first SDM stage is the dominant one, we must have

$$2^{(n_1-n_2)} < \frac{\frac{5}{R} - \frac{2}{\pi}\sin(\frac{2\pi}{R})}{\frac{14}{R} - \frac{9}{\pi}\sin(\frac{2\pi}{R}) + \frac{1}{\pi}\sin(\frac{4\pi}{R})}, \tag{19}$$

i.e., $n_1 - n_2 \le 2$. In practice, n_2 is chosen to be as small as possible (usually 1) to minimize the hardware cost. This leads to the 3-bit resolution limit of the quantizer at the dominant SDM stage in our SSMB.

D. Multiple-Stage Multiple-Bit Scheme (MSMB)

High-resolution applications can be achieved by using the multiple-stage multiple-bit (MSMB) scheme. Different from the FSMB scheme, MSMB is a high-resolution SDM using multiple-bit technique at more than one stage under the prescribed design rules. In MSMB, the total power distortion in (14) is successively approximated by the succeeding $\xi_{E_i}^t$, $1 \le i \le M$, until the required resolution has been met. The goal is to make the total noise power in (14) meet the specification while keeping (8) valid.

Take the CAFO SDM discussed above as an example. The MSMB starts by determining the pivot SDM stage, say the p-th stage. The stages after the pivot stage (including the pivot stage) have one-bit representation for their intermediate quantized outputs, Y_k, $p \le k \le M$, and for each of the stages before the pivot stage, we increase two bits stage by stage, from the pivot stage on. The number is determined by (19). By doing so, the relationship of (8) can be kept to validate our approximation from the starting stage. Let n_i, $1 \le i \le M$ be the number of bits used to represent the intermediate quantized output Y_i in the i-th stage. For an MSMB with a pivot stage p, we have

$$n_i = \begin{cases} 1 + 2 * (p - i) & ;\ for\ 1 \le i < p \\ 1 & ;\ for\ p \le i \le M. \end{cases} \tag{20}$$

The pivot p is chosen to be the maximal p which meets the required resolution

$$TSNR_p = \frac{\xi_{signal}}{\sum_{i=1}^{p} \xi_{E_i}^t} > TSNR_{required}. \tag{21}$$

Selection of a suitable pivot can be accomplished with the aid of (7) and (14).

IV. Simulation Results

Extensive behavioral model simulations are made to verify our multiple-bit schemes. The analysis example used is the 7-th order CAFO SDM suffering from non-ideal effects as discussed above. The analog input $X(z)$ is a pure oversampled sinusoidal signal with a frequency of $\frac{1}{8}$ of the Nyquist frequency whose amplitude varies from 0.1 to 1.1, normalized to the single-bit quantization step. The oversampling ratio is chosen to be 16 [16].

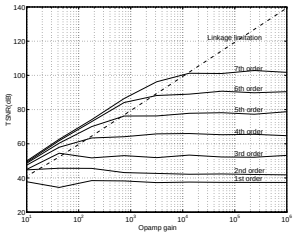
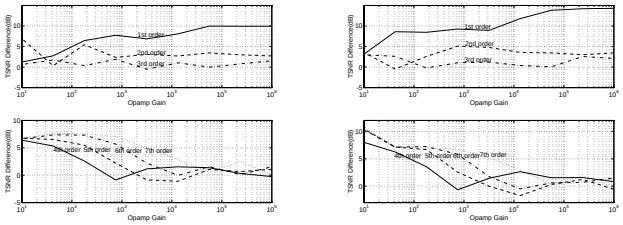


Fig. 4. TSNR of CAFO 2-bit SSMB SDM.



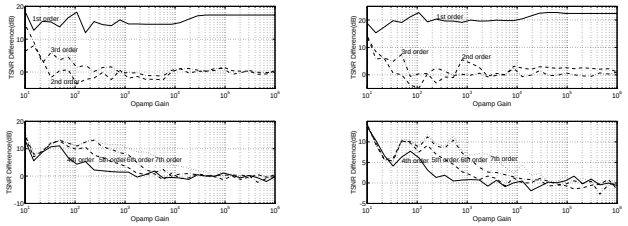
(a) (b)

Fig. 5. TSNR difference of (a)2-bit SSMB, (b)3-bit SSMB and that of conventinal ASB SDM.

A. The SSMB SDM

We first discuss the leakage noise due to a finite op-amp gain, ξ_{Ei}^{fg}.

1. *A 2-bit SSMB SDM:* A 2-bit quantizer is used at the first SDM stage. Fig. 4 is the simulation results of TSNR (solid lines) from the 1-st to the 7-th order CAFO SDMs. The dashed line marked by "Leakage limitation" is the result obtained by directly applying (18). It gives a close prediction about the effects of leakage limitation except there is a 6dB underestimation.
   Given a finite op-amp gain, noise from the dominant leakage error dominates those of the others. SSMB scheme successfully compensates the dominant leakage noise by using a 2-bit quantizer at the dominant stage shown by our simulation results for the op-amp gain of less than 10,000. Note that for the op-amp gain larger than 10,000, our SSMB scheme seems to be invalid. The reason is that for a sufficiently large op-amp gain, the intermediate leakage error noises are small enough to be neglected. Instead, the intrinsic quantization error noise dominates all the leakage ones. Under such a situation, the SDM is virtually considered to be near-ideal which needs no multiple-bit compensation. The same situation happens in conventional all-single-bit (ASB) CAFO SDM; however, the near-ideal op-amp gain limit for the 2-bit SSMB SDM is less than that of the ASB SDM which is about 30,000 [16]. That is, SSMB does help in loosening the specification of the circuits.
   Moreover, the SSMB scheme is especially suited to high-order SDM applications. Fig. 5(a) depicts the TSNR enhancement of our 2-bit SSMB SDM compared with the ASB SDM. An enhancement is observed in the region where the approximation of the dominant leakage error noise is valid (see Fig. 4).
   In the first-order case, there is no leakage error. The first-order SDM directly gains the advantage of small quantization steps. Therefore, 2-bit SSMB SDM always provides more TSNR than ASB SDM. It seems that the smaller quantization steps also help reducing the harmonic distortions and give an extra improvement on its TSNR.
   In the second and the third order cases, the intrinsic quantization error is compatible with the leakage errors since they inherently provide small TSNRs under a small oversampling ratio; consequently, the enhancement of TSNR is not significant.
   As the order goes up to four and above, an enhancement of up to 6dB is observed from the simulation results which therefore justifies (18). Note that SSMB scheme is more efficient in high-order and low op-amp gain applications where the leakage errors are significant.
2. *A 3-bit SSMB SDM:*Similar results are seen by a 3-bit SSMB SDM. Intuitively, we expect there is 12dB TSNR enhancement, but the results are consistent with our prediction only where the opamp gain is less than 50 as shown in Fig. 5(b). The reason is that 3-bit SSMB has ξ_{E1}^{fg} compatible with ξ_{E2}^{fg}. As a result, ξ_{Ei}^{fg} no longer dominates the leakage noises and (18) becomes invalid.
3. *The 4-bit and 5-bit SSMB SDM:* The TSNR enhancement of a 4-bit SSMB SDM is shown in Fig. 6(a). Compared with Fig. 5(b), we can see that 4-bit SSMB SDM improves TSNR by 12dB. In fact, ξ_{E2}^{fg} becomes larger than ξ_{E1}^{fg}. If the resolution of the quantizer at the first SDM stage continuously increases, the dominating leakage noise will be ξ_{E2}^{fg} rather than ξ_{E1}^{fg}. Therefore, no more TSNR improvement will be observed. Fig. 6(b) illustrates the TSNR improvement of a 5-bit SSMB SDM which is no more than that of the 4-bit SSMB.



(a) (b)

Fig. 6. TSNR difference of (a)4-bit SSMB, (b)5-bit SSMB and that of ASB SDM.

We now discuss the leakage noise due to the capacitor mismatch, $\xi_{E_i}^{cv}$. Though not as important as that caused by the finite op-amp gain [16], the leakage noises due to the capacitor mismatch are discussed for completeness. Fig. 7

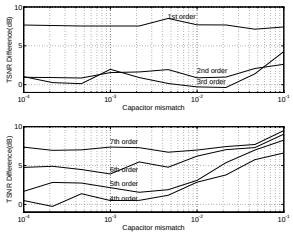
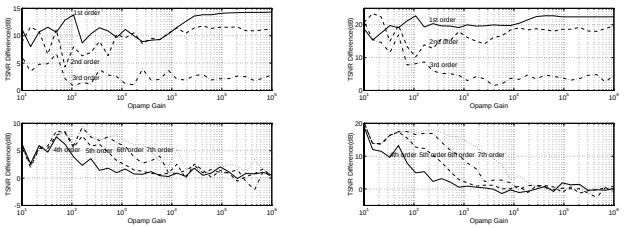


Fig. 7. Comparing the TSNR of CAFO 2-bit SSMB SDM with that of the ASB SDM when capacitor mismatch is considered. The op-amp gain is set to 1,000.



(a) (b)

Fig. 8. TSNR difference of (a)(3,2) MSMB, (b)(5,3) MSMB and that of ASB SDM.

is the TSNR enhancement of the 2-bit SSMB SDM over the ASB one where the op-amp gain is 1,000. It can be seen that for a small value of capacitor mismatch ($|\Delta G| \leq 5 \times 10^{-3}$), the improvement is the same as that in Fig. 4 due to the dominance of $\xi_{E_1}^{fg}$. Alternatively, a larger improvement can be observed for a larger capacitor mismatch ($|\Delta G| > 10^{-2}$) since ξ_{E1}^{cv} levels with $\xi_{E_1}^{fg}$. Under such a condition, the multiple-bit scheme can alleviate both leakage error noises simultaneously.

B. The MSMB SDM

Figs. 8(a) and 8(b) show the simulation results of the TSNR enhancement of the (3,2) and (5,3) MSMB schemes. A (3,2) MSMB SDM is a CAFO SDM with a 3-bit quantizer and a 2-bit quantizer at the first and second stages, respectively, while the rest of the stages use one-bit quantizers. Similarly, a (5,3) MSMB SDM has a 5-bit and a 3-bit quantizers at the first two stages.

The simulation results depicted in Fig. 8(a) show that a (3,2) MSMB SDM behaves as a 3-bit SSMB SDM with respect to the TSNR enhancement, though it is inherently a sophisticated design trying to alleviate $\xi_{E_2}^{fg}$ in order to expect a better performance. It fails since it does not obey our design rules.

On the other hand, a (5,3) MSMB SDM, which follows the prescribed MSMB design rules in the context, exhibits 20dB TSNR improvement. Comparing with Fig. 6(b), it is more effective than 5-bit SSMB.

V. Conclusion

Based on the CIQE high-order SDM architecture, multiple-bit schemes are proposed to compensate for the non-ideal circuit effects, such as the finite op-amp gain and the capacitor mismatch, and shown to be valid via simulations. The SMB scheme is used when the leakage errors are not significant which is usually for the SDM with a low order and a high oversampling ratio; while the SSMB scheme is well suited to the high-order SDM operating under a low-oversampling ratio. For extremely high-resolution applications, the MSMB scheme is an appropriate approach.

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