Low-Power Multiple-Valued Current-Mode Integrated Circuit with Current-Source Control and Its Application

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Abstract– A new current-source control technique is proposed to design a low-power high-speed multiple-valued current-mode (MVCM) integrated circuit in a low supply voltage. The use of a differential logic circuit (DLC) with a pair of dual-rail inputs makes the input voltage swing small, which results in a high driving capability at a lower supply voltage, while having large static power dissipation. In the proposed DLC using switched current control, the static power dissipation is greatly reduced because current sources in non-active circuit blocks are switched off. In the current control, no additional transistors are required to control the current sources because a current-control circuit is already used in the threshold detector. As a typical example of arithmetic circuits, a new 1.5V-supply 54×54-bit multiplier based on a $0.8\mu m$ standard CMOS technology is also designed. Its performance is about 1.3 times faster than that of a binary fastest multiplier under the normalized power dissipation.

I. Introduction

The emerging trend of decreasing power dissipation in a single chip has been rapidly increased in the present deep submicron ULSI technologies. Low power dissipation can be achieved by reducing a supply voltage, capacitance and the number of the active devices to perform a given function[1]-[3]. Multiple-valued current-mode (MVCM) integrated circuits have a potential advantage to reduce the wiring complexity and the number of active devices in arithmetic large-scale-integration chips because the frequently used linear sum operation can be performed simply by wiring[4]-[6]. In fact, several arithmetic integrated circuits have been designed and fabricated by the combination of MVCM logic circuits, resulting in better performance compared with the corresponding binary implementation[7].

Threshold detector is one of the most important building blocks in MVCM integrated circuits because the operating speed is determined by the switching delay of the threshold detector. To improve the switching delay of a multiple-valued basic component in a lower supply voltage, a threshold detector based on differential logic has been proposed[8]. This threshold detector requires a pair of complementary current signals for the dual-rail operation. Using the dual-rail complementary inputs, the NMOS transistor to produce the output current in the threshold detector is always turned on. Thus the input voltage swing becomes smaller and the switching speed of the circuit can be improved even if a low supply voltage is used.

However, the power dissipation of the threshold detector based on differential logic remains constant because a constant current always flows in a source-coupled pair of transistors. Therefore, the static power dissipation is increased in a multiple-valued current-mode logic circuits.

This paper presents a new MVCM logic circuit to reduce the static power dissipation with high-speed switching capability and a low supply voltage. In the proposed MVCM logic circuit, each current source is turned off when it is not active, which makes the static power dissipation zero. Since the current sources in differential logic circuits (DLCs) are directly controlled by changing the gate voltage of a current source, critical path is not increased in the proposed MVCM logic circuit, which keeps high-speed operations with lower power dissipation.

As an application, a 54×54-bit multiplier with a 1.5V supply voltage is designed based on a 0.8-μm standard CMOS technology. As a result, the power dissipation of the proposed multiplier can be reduced to less than 20% of a conventional multiple-valued one with keeping the same multiplication speed. In addition, under the same power dissipation with the supply voltage of 1.5V, the operating speed of the proposed multiplier is 1.3 times faster than that of a binary CMOS multiplier.

II. Basic Low-Power MVCM Logic Circuit

In MVCM logic circuits, threshold detection is one of the most important functions. It is well-known that the operating speed of any MVCM logic circuits is primarily limited by the delay of the threshold detectors. Especially, it is strongly requested that high-speed operations must be performed in MVCM logic circuits even at lower power dissipation. In the following section, we discuss how to reduce the power dissipation of the threshold detector with keeping a high-speed switching capability.

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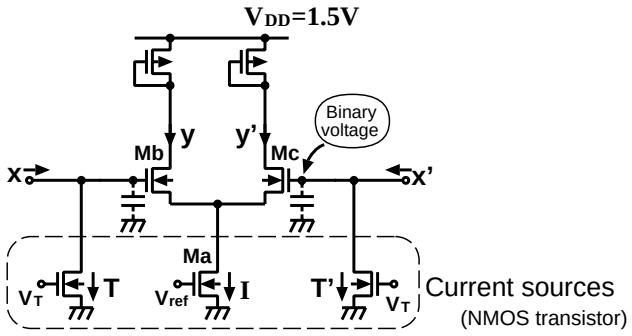

Figure 1: Threshold detector.

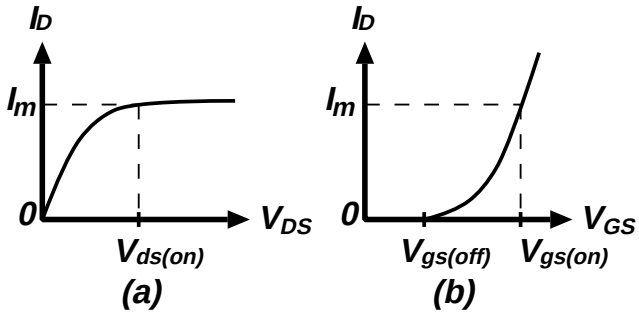

Figure 2: I_d-V_{ds} characteristics: (a) I_d-V_{ds} characteristic of Ma. (b) I_d-V_{ds} characteristic of Mb and Mc.

A. Delay of a threshold detector with a DLC

Figure 1 shows a threshold detector based on a DLC where three pairs of dual-rail complementary input signals, threshold signals and output signals are represented as (x, x'), (T, T') and (y and y'), respectively. In R-valued logic, these pairs of the complementary signals satisfy the following equations:

$$x + x' = R - 1 \quad (1)$$

$$T + T' = R - 1 \quad (2)$$

$$y + y' = m \quad (3)$$

where $+$ and $-$ indicate an arithmetic addition and a subtraction, respectively, and where the output current $m \in \{0, 1, \cdots R-1\}$.

If the current-source transistor M_a has the $I_d - V_{ds}$ characteristic shown in Fig.2(a), and both the source-coupled transistors M_b and M_c have the $I_d - V_{gs}$ characteristic shown in Fig.2(b), then the input voltage swing can be reduced in the switched current source based on a DLC. The output current I_m is controlled by the source-coupled pair of M_b and M_c with the dual-rail complementary inputs. Since either M_b or M_c is always turned on, m is always flowing through M_a. The input voltage swing ΔV to switch the current m is given by

$$\Delta V = V_{gs(on)} - V_{gs(off)}. \quad (4)$$

Equation (4) indicates that the input voltage swing for the threshold detector becomes independent from the switching voltage $V_{ds(on)}$ in the current-source transistor M_a. As a result, the supply voltage V_{DD} can be reduced for the same driving current m, so that the switching speed of the proposed threshold detector becomes high at a low supply voltage.

However, the power dissipation in the threshold detector remains constant even when the circuit is not active. To solve this problem, we discuss about a switched current control technique for power saving.

B. Design of a low-power MVCM logic circuit

Figure 3 shows the current-source control scheme of the proposed MVCM logic circuit. To reduce the power dissipation, the current of non-active threshold detectors is cut off, which greatly reduces the power dissipation with keeping high-speed operation capability.

Figure 4 shows the principle of current-source control with no-additional active devices. A constant current in a DLC flows even when the circuit is not active as shown in Figure 4(a). When the current source is turned off, the current is cut off as shown in Figure 4(b). Consequently, the gate of the current source is controlled by

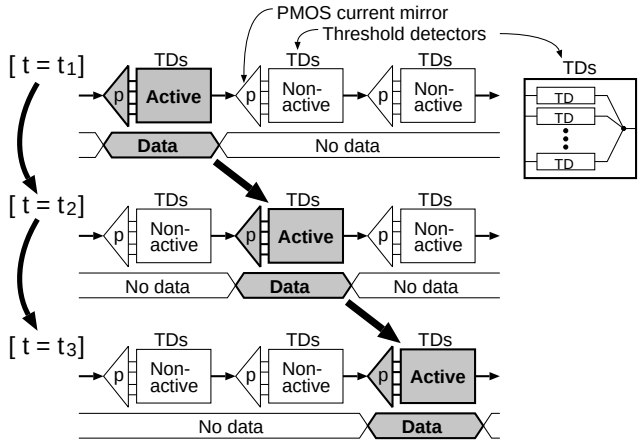

Figure 3: Current source control in a proposed MVCM circuit.

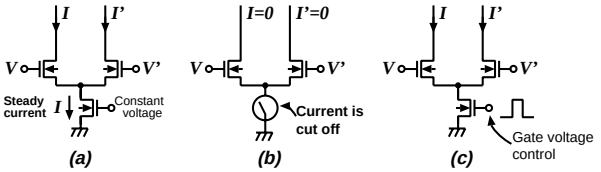

Figure 4: Switched-current differential logic circuit: (a) Conventional current-mode circuit, (b) Cut-off mode (c) Current-source control without active devices.

	V_a	V_b	V_c	V_d	V_e	V_f
Block A "Active"	*High*	*High*	*Low*	*Low*	*Low*	*Low*
Block B "Active"	*Low*	*High*	*High*	*High*	*Low*	*Low*
Block C "Active"	*Low*	*Low*	*Low*	*High*	*High*	*High*

Figure 6: Gate-voltage states of current sources.

the external signal as shown in Figure 4(c). Using the above control scheme, the power dissipation of a DLC can be greatly reduced without any increased critical path by direct gate-voltage control of the current source.

In case of the cascade connection of several threshold detectors, the power dissipation can be reduced by the same current-source control technique shown in Figure 4. Figure 5 shows the three-stage cascade connection of the threshold detectors. When the transistors of the current sources $M1$ and $M2$ are turned off and a pair of the input currents (x, x') is zero, the charge levels on the gates of the transistors $M4$ and $M5$ are still kept on the gate capacitances, respectively. Since a pair of the output currents (y, y') depends on the binary voltages on the gates of $M4$ and $M5$, the output currents remain unchanged. Moreover, the current sources M_6-M_8 and M_9-M_{11} are turned on and off, respectively. Using the above current-source control, only the block B becomes active, which makes the power dissipation of the MVCM logic circuit lower with keeping the short critical path.

Figure 6 shows the current-source control scheme to perform the operation shown in Figure 3. Using this scheme, large-scale MVCM logic circuits can be also operated at low power dissipation without using additional circuits.

III. Design of a low-power multiplier

As a typical application of MVCM logic circuits, we consider a design of SD arithmetic circuits.

A. Radix-2 SD addition algorithm

As a typical application of arithmetic circuits, a high-speed signed-digit(SD) multiplier can be designed. The radix-2 SD number representation using a symmetrical digit set $\{-1, 0, 1\}$ is defined as follows[9]:

$$X = (x_{n-1} \cdots x_1 x_0) = \sum_{i=0}^{n-1} x_i \cdot 2^i \qquad (5)$$

where $x_i \in \{-1, 0, 1\}$. The redundancy allows totally parallel arithmetic operations.

The addition of two numbers, $A = (a_{n-1} \cdots a_1 a_0)$ and $B = (b_{n-1} \cdots b_1 b_0)$, where $a_i, b_i \in \{-1, 0, 1\}$, is performed by three successive steps in each digit:

$$z_i = a_i + b_i \qquad (6)$$

Table 1: 3-valued current level.

Logic value	**-1**	**0**	**1**
$\mathbf{a_i,\ b_i,\ w_i,\ c_i,\ s_i}$	**0**	$\mathbf{I_0}$	$\mathbf{2I_0}$
$\mathbf{a_i',\ b_i',\ w_i',\ c_i',\ s_i'}$	$\mathbf{2I_0}$	$\mathbf{I_0}$	**0**

I_0 : Unit currret

Table 2: 5-valued current level.

Logic value	**-2**	**-1**	**0**	**1**	**2**
$\mathbf{z_i}$	**0**	$\mathbf{I_0}$	$\mathbf{2I_0}$	$\mathbf{3I_0}$	$\mathbf{4I_0}$
$\mathbf{z_i'}$	$\mathbf{4I_0}$	$\mathbf{3I_0}$	$\mathbf{2I_0}$	$\mathbf{I_0}$	**0**

$$2c_i + w_i = z_i \qquad (7)$$

$$s_i = w_i + c_{i-1} \qquad (8)$$

where the linear sum $Z = (z_{n-1} \cdots z_1 z_0)$, the intermediate sum $W = (w_{n-1} \cdots w_1 w_0)$, the carry $C = (c_{n-1} \cdots c_1 c_0)$ and the final sum $S = (s_{n-1} \cdots s_1 s_0)$ are $z_i \in \{-2, -1, 0, 1, 2\}$, $w_i \in \{-1, 0, 1\}$, $c_i \in \{-1, 0, 1\}$ and $s_i \in \{-1, 0, 1\}$, respectively.

To retain the final sum s_i within the set $\{-1, 0, 1\}$, c_i and w_i are determined by z_{i-1} together with z_i as follows:

$$\begin{cases} c_i = 1 & w_i = 0 & \text{if } z_i = 2 \\ c_i = 1 & w_i = -1 & \text{if } z_i = 1 \text{ and } z_{i-1} \geq 1 \\ c_i = 0 & w_i = 1 & \text{if } z_i = 1 \text{ and } z_{i-1} < 1 \\ c_i = 0 & w_i = 0 & \text{if } z_i = 0 \\ c_i = 0 & w_i = -1 & \text{if } z_i = -1 \text{ and } z_{i-1} \geq 1 \\ c_i = -1 & w_i = 1 & \text{if } z_i = -1 \text{ and } z_{i-1} < 1 \\ c_i = -1 & w_i = 0 & \text{if } z_i = -2. \end{cases} \qquad (9)$$

The final sum is independent of the word length n because the carry-propagation chain is limited to one digit to left[10]. Therefore, the addition speed of the SD adder is higher than that of ordinary binary adders.

B. Structure of a low-power SD multiplier

In the proposed MVCM logic circuits, each digit of the above SD numbers corresponds to a pair of complementary current signals. The adder inputs, the intermediate sum, the carry and final sum are represented as (a_i, a_i'), (b_i, b_i'), (w_i, w_i'), (c_i, c_i') and (s_i, s_i'), respectively, which is given by Table 1. Similarly, the linear sum (z_i, z_i') is shown in Table 2.

The radix-2 SD adder can be designed as shown in Figure 7. The linear summation of Eqs.(6) and (8) can be obtained by wiring without active devices. The operation of Eq.(7) is

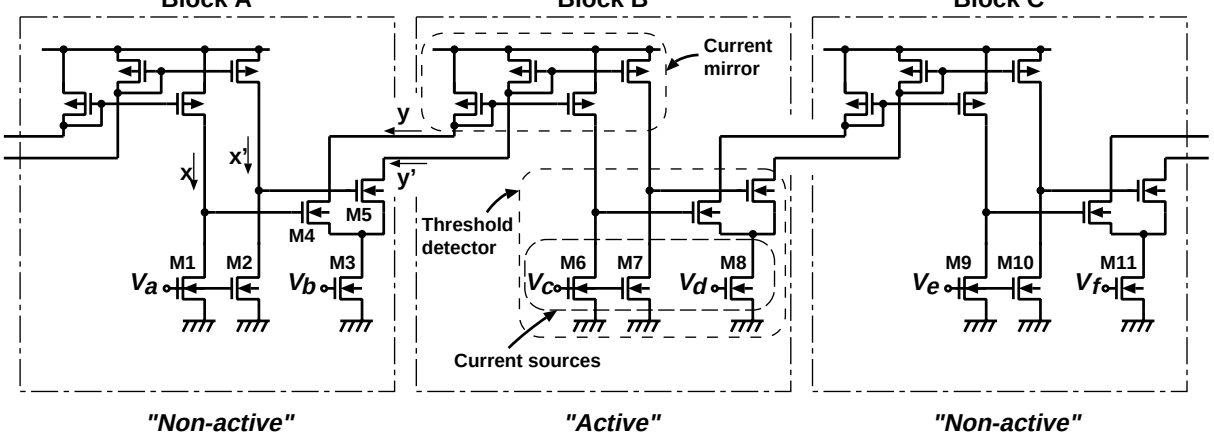

Figure 5: Cascade connection of three threshold detectors.

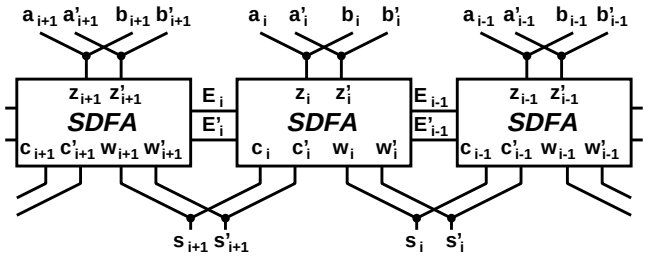

Figure 7: radix-2 SD adder.

Table 3: 5-valued threshold current level.

Threshold value	-0.5	-1.5	0.5	1.5
T	$0.5I_0$	$1.5I_0$	$2.5I_0$	$3.5I_0$
T'	$3.5I_0$	$2.5I_0$	$1.5I_0$	$0.5I_0$

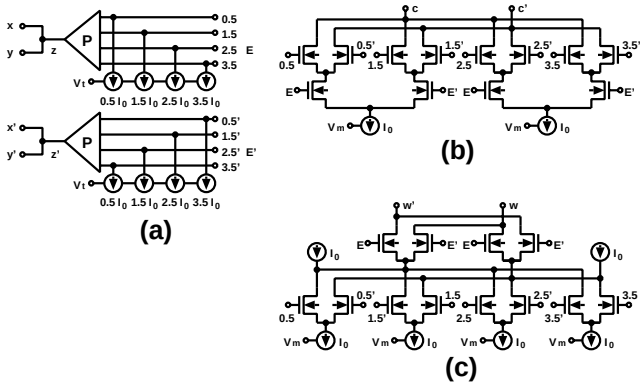

Figure 8: Circuit configuration of the SDFA.

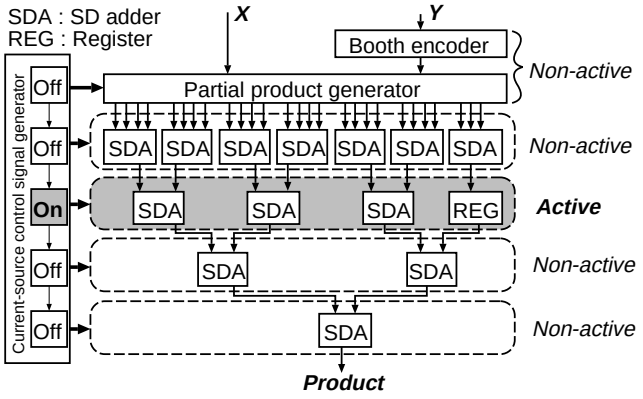

Figure 9: Block diagram of the 54×54b multiplier.

performed with an SD full adder (SDFA). E_i and E_i' are used as the control signals to give the conditions of $z_{i-1} \geq 1$ and $z_{i-1} < 1$ in Eq.(9). z_i and z_i' takes five values which are detected four kinds of the comparators as shown in Table 3. As a result, the circuit configuration of the SDFA is designed by 50 MOS transistors shown in Figure 8.

A low-power multiple-valued multiplier is designed using the SDFAs as shown in Figure 9. Using the Booth algorithm, 27 partial products for 54-b multiplication are generated from the partial product generator. Since SD addition can be performed by a binary-adder-tree scheme, 27 partial products are added in parallel by just four addition stages. Because of the proposed switched-current control scheme for low-power current-mode circuits, only one of five divided stages in the multiplier is controlled to be activated.

As shown in Figure 10, clock distribution in the proposed 54-b multiplier is also proposed to compensate the performance of high-speed multiple-valued current-mode arithmetic operations. Due to the regular structure of the SD multiplier, clock skew can be controlled to be minimized. The hardware overhead for the above clock distribution is less than 20% of total transistors in the multiplier.

C. Application to matrix-vector multiplication

In the proposed multiplier, the input and the output words are represented by binary and signed-digit data formats, respectively, so that it

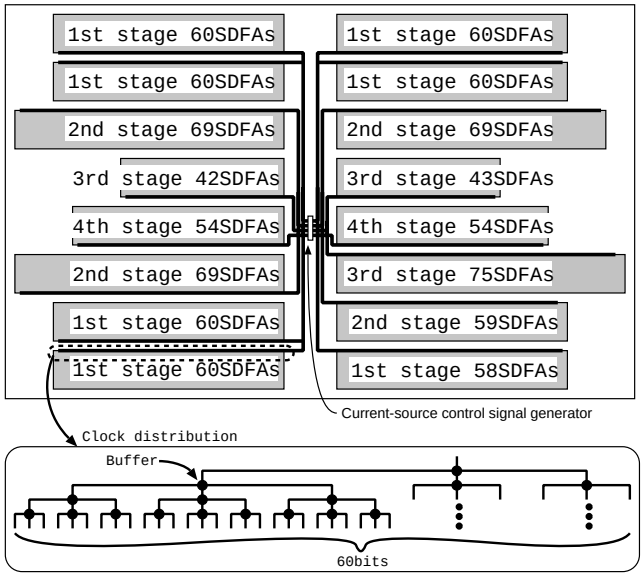

Figure 10: Floor plan of the proposed 54-b multiplier.

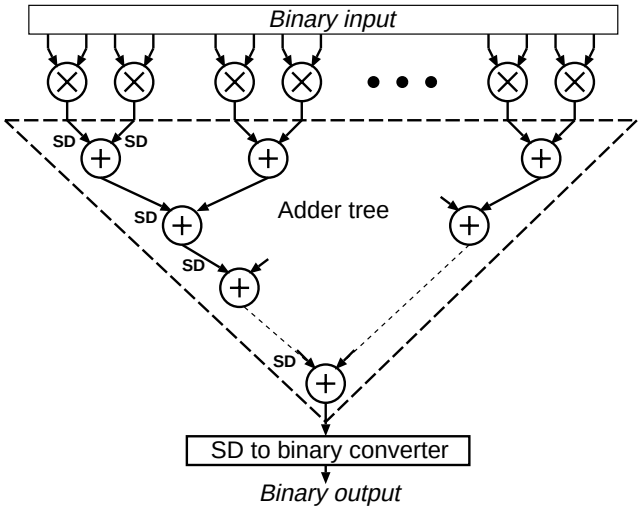

Figure 11: Matrix-vector multiplication.

is suited to perform the multi-operand multiply-addition operations. Figure 11 shows a block diagram for the matrix-vector multiplication using multipliers, an adder tree and an SD-to-binary converter. After the multiplications in the first stage, signed-digit number representation is used in the adder tree. At only the final stage, signed-digit number representation is converted into binary one to connect with the conventional binary system. Consequently, the delay overhead for data conversion is negligible in the application to such large-scale multi-operand multiply-addition operations.

IV. Evaluation

Figure 12 shows the simulated waveforms of currents in three cascaded threshold detectors using PSPICE simulation. The power dissipation

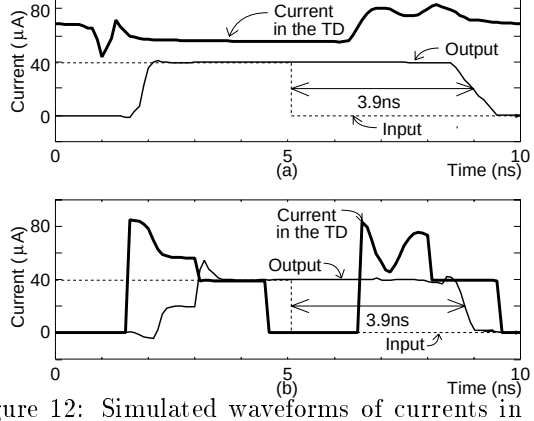

Figure 12: Simulated waveforms of currents in cascaded threshold detectors: (a) Output current and total current in the conventional circuit, (b) Output current and total current in the proposed circuit.

Figure 13: Photomicrograph of an SDFA.

of the proposed circuit is less than 60% compared with that of the conventional circuit, while the switching speed is almost comparable each other.

Figure 13 shows a photomicrograph of the SDFA fabricated in a standard 0.8-μm CMOS technology. The effective chip size is $77 \times 70(\mu m^2)$. The small SDFA design based on multiple-valued logic is useful for the reduction of the total chip area. Figure 14 shows the measured wave forms in the proposed circuit, where V_T and V_{ref} are gate voltages of the current source transistors. The basic operation using the current-source control is confirmed from the experimental result.

Table 4 summarizes the performance of the proposed multiplier together with those of a conventional multiplier and a binary CMOS multiplier by PSPICE simulation whose parameters are normalized under a 0.8-μm standard CMOS technology. Since the proposed multiplier is divided into five parts, only one part is controlled to be activated. As a result, the power dissipation of the proposed multiplier can be reduced to less than 20% of a conventional multiple-valued one under the condition of the same multiplication time. If the word length of input data is longer in the proposed multiplier, its power dissipation becomes much less because less transistors are activated. Moreover, under the same power

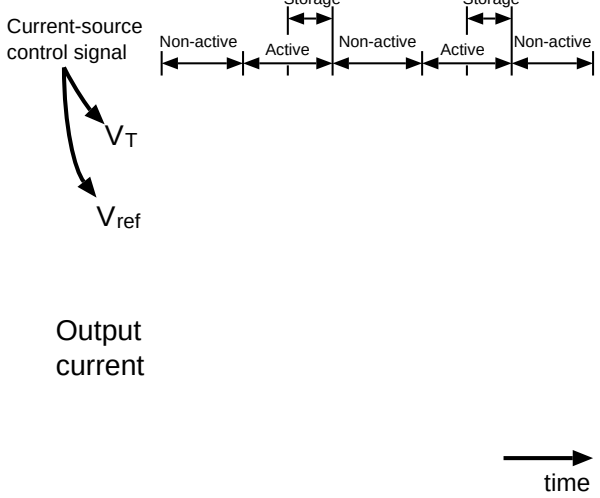

Figure 14: Measured waveforms of the SDFA.

Table 4: Comparison of multipliers.

	Binary * CMOS	Conventional MVCM	Proposed MVCM
Supply voltage	1.5v	1.5v	1.5v
Delay	16ns	12ns	12ns
Power dissipation	0.19W	1.0W	0.19W
Chip area	———	43.2mm^2	45.1mm^2

PSPICE simulation based on a 0.8μm CMOS technology

* H.Makino,Y.Nakase and H.Shinohara, "An 8.8ns 54¡ 54-bit Multiplier Using New Redundant Binary Architecture," IEEE Proc. Int'l Conf. Computer Design, pp.202-205, 1993.

dissipation with the supply voltage of 1.5V, the operating speed of the proposed multiplier is 1.3 times faster than that of a binary CMOS multiplier. Since the current-source control signal generator is designed by the combination of standard CMOS gates, its power dissipation is less than 2.6% of total power dissipation.

V. Conclusion

A new threshold detector using a switched current control technique has been presented to reduce the static power dissipation in the MVCM logic circuit. The use of switched current control technique in the source-coupled logic circuit makes the static current flow cut off, so that the static power dissipation becomes zero in this circuit. Since the above power-saving operation is easily performed by controlling the gate voltage of the current source in the source-couple logic, there is no hardware overhead for the static power saving. Moreover, the use of dual-rail source-coupled logic circuits makes the input voltage swing small, so that high-speed operations can be performed at a low supply voltage. As a typical application to large-scale arithmetic systems, it is demonstrated that the maximum operating delay of the proposed 54×54-b multiple-valued multiplier is evaluated to be about 12 (nsec) by PSPICE simulation based on a $0.8-\mu m$ standard CMOS technology at a supply voltage of 1.5V, whose performance is superior to that of a corresponding binary one.

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