Modeling and Detection of Dynamic Errors due to Reflection- and Crosstalk-Noise

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Abstract – A new algorithm for the generation of test sequences to detect dynamic errors due to reflection and crosstalk noise in combinational circuits is presented. Based on the circuit level a new approach for error modeling including the duration of reflection and crosstalk errors, is described. The presented algorithm takes the high influence of error durations as well as gate and transmission line delays on the testability into account.

I. Introduction

A powerful approach to handle signal integrity problems during the layout design phase of digital high-speed components is offered by the method of multi level simulation (gate level/circuit level). In order to use these simulations effectively, appropriate stimuli sequences are necessary. Searching for these stimuli sequences is equivalent to the test generation problem. Therefore, in this paper we present a new algorithm for the generation of test sequences to detect dynamic errors due to reflection and crosstalk noise in combinational circuits. Compared to others ([1], [2], [3]) our approach for error modeling also includes the uncertainty about a logic state due to reflection or crosstalk noise as well as an estimation of the error duration. Furthermore, coherences between error durations and gate and transmission line delays concerning the testability of the above mentioned dynamic errors are taken into account within the algorithm.

The rest of the paper is organized as follows: In Section II logic models for the characterization of reflection and crosstalk errors are derived. Based on these models, the essential features of the developed algorithmic test generation method are described in Section III. In Section IV an example is discussed. Finally conclusions and a summary are given in Section V.

II. Error Modeling

Inside a transmission line network reflections occur at line discontinuities (e.g. vias, jogs, branches) and at unmatched line terminations, located at the connections of I/O-stages of digital circuits. Crosstalk noise can appear between two or more electromagnetically coupled transmission line networks [4]. Analyzing crosstalk noise, a possible superposition of reflection noise has also to be taken into account.

From the exploration of the typical reflection behavior inside a transmission line network N at the circuit level [5], a reflection error model is derived at the logic level (s. Fig. 1). This model describes an expected uncertainty of the value of a logic variable $j(t)$ due to reflection noise at a gate input j connected to the mentioned net N:

$$j(t) \xrightarrow[transition\ at\ i \in N]{} j_{E_r}(t) = \begin{cases} j(t); & t < t_{trans} + \Delta t_{ij} \\ E_r\ ; & t_{trans} + \Delta t_{ij} < t < t_{trans} + \Delta t_{ij} + \Delta t_{E_r} \\ j(t); & t > t_{trans} + \Delta t_{ij} + \Delta t_{E} \quad . \end{cases} \tag{1}$$

Within relation (1) t_{trans} is the point in time of a transition at input i of net N, Δt_{ij} is the delay parameter between nodes i and j of net N, and Δt_{E_r} is the length of the time interval in which the value of $j(t)$ is uncertain (duration of the reflection error E_r).

From the exploration of the typical crosstalk behavior of two coupled nets N and N' at the circuit level [5], a crosstalk error model can be derived at the logic level (s. Fig. 2). It describes an expected uncertainty of the value of the logic variable $j'(t)$ due to crosstalk (and reflection) noise at a gate input j' of net N': [1]

$$j'(t) \xrightarrow[transition\ at\ i \in N]{} j'_{E_c}(t) = \begin{cases} j'(t); & t < t_{trans} + \Delta t_{ij'} \\ E_c\ ; & t_{trans} + \Delta t_{ij'} < t < t_{trans} + \Delta t_{ij'} + \Delta t_{E_c} \\ j'(t); & t > t_{trans} + \Delta t_{ij'} + \Delta t_{E_c} \quad . \end{cases} \tag{2}$$

Within relation (2) t_{trans} is the point in time of a transition at input i of net N, $\Delta t_{ij'}$ is the delay parameter between node i of net N and node j' of net N', and Δt_{E_c} is the length of the time interval in which the value of $j'(t)$ is uncertain (duration of the crosstalk error E_c).

[1] The modeling of crosstalk effecting from N' to N or among more than two nets is similar.

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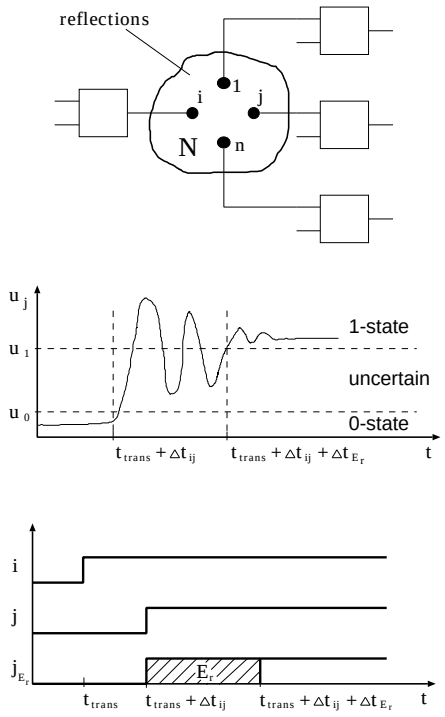

Fig. 1. Relationships of reflection error modeling

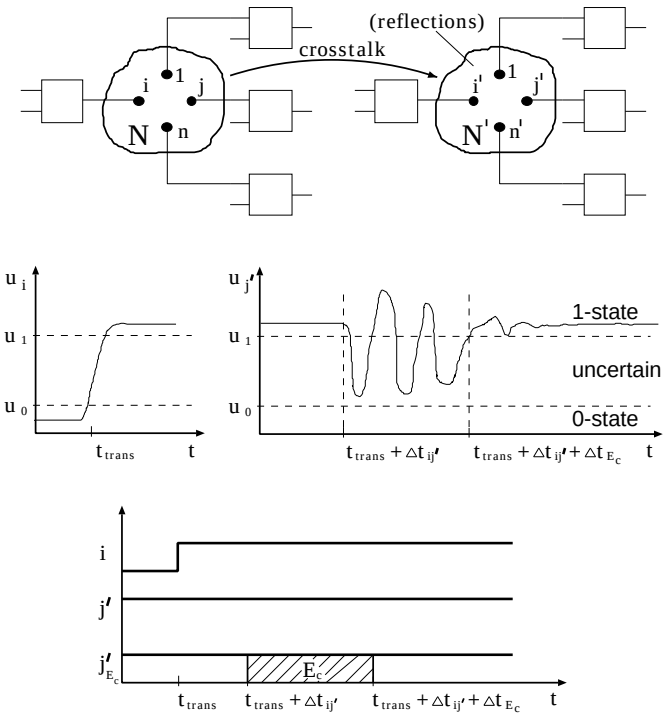

Fig. 2. Relationships of crosstalk error modeling

III. Test Generation Algorithm

Stimulation, propagation, and compensation of reflection or crosstalk errors is highly influenced by timing. Therefore, the gate and transmission line delays as well as the error durations have to be taken into account during the test generation.

In the following, a combinational circuit C is considered. If there is a set of test sequences $\{(S)_{real}\}$ detecting an expected reflection or crosstalk error in the circuit *with delays* (C_{real}), then it is a subset of a set of test sequences $\{(S)_{ideal}\}$ detecting the same error in the circuit *without delays* (C_{ideal}): $\{(S)_{real}\} \subset \{(S)_{ideal}\}$. Therefore the following strategy to solve the test problem is deduced:

1. Find a stimuli sequence $(S) \in \{(S)_{ideal}\}$.
2. Check whether it is $(S) \in \{(S)_{real}\}$.

This strategy is used by the new test generation algorithm. The algorithm initiates from a gate level description of the digital circuit to be tested. All gates are assumed to be error-free. The sites of expected errors are only located inside the transmission line networks interconnecting the gates. The algorithmic procedure for the generation of $\{(S)_{ideal}\}$ is based on a branch and bound strategy [6]. Based on the error models described in Section II, it is assumed that each line termination in C takes one of the logic values listed in Table I. In Fig. 3 the branch and bound policy and the control flow of the algorithm are shown [2].

[2] A more detailed description of the algorithm is given in [7].

TABLE I
Logic Values used with the Algorithmic Test Generation

logic value	meaning
$(0,0)$	permanent '0'
$(1,1)$	permanent '1'
$(0,1)$	(0,1)-transition
$(1,0)$	(1,0)-transition
(x,x)	not assigned
E_r	reflection error
E_c	crosstalk error

A. Computation Time

Algorithmic test generation for the detection of static errors (e.g. stuck-at errors) is often based on branch and bound processes with $k = 2^n$ possible states to be chosen at n primary inputs. The computation time Δt_{bb2} to determine test patterns that inherit such algorithms is usually explored by benchmarks with standard circuits given by F. Brglez (e.g. [8]). However, to the authors knowledge there are no standard benchmarks for the detection of dynamic errors. Therefore, we give a worst-case estimation of the computation time our algorithm requires. The generation of test sequences for the detection of reflection and crosstalk errors has to handle $k^2 = 4^n$ states to be possibly chosen at the n primary inputs (s. Decision Tree in Fig. 3). Hence, the computation time Δt_{bb4} to determine the test sequences may be estimated by $\Delta t_{bb4} = (\Delta t_{bb2})^x$ whereby $1 < x < 2$.

IV. Example

As an example a 3-bit-adder circuit is considered. The gate level description (s. Fig. 4) includes gate and transmission line delays. Line 3 and line 5 of the adder circuit are partially electromagnetically coupled as depicted in Fig. 4. With the occurrence of a transition at the primary input 3 a crosstalk error at the input A of gate 8 may be expected. The set of test sequences $\{(S)_{real}\} \subset \{(S)_{ideal}\}$ detecting the expected crosstalk error is shown in Table II.

In order to demonstrate the dependencies between error propagation, its compensation, and the timing, an error simulation with the stimuli sequences

1. $(S)_1 = ((0,0),(0,0),(0,1)) \in \{(S)_{real}\} \subset \{(S)_{ideal}\}$ and
2. $(S)_2 = ((1,0),(1,0),(1,0)) \in \{(S)_{ideal}\} \setminus \{(S)_{real}\}$

has been performed. Fig. 5 shows the simulation results. The first crosstalk error stimulated by $(S)_1$ at the point in time $t_{trans1} = 10ns$ occurres at the point in time $t'_{E_c} = t_{trans1} + \Delta t_{control} + \Delta t_{ij'} = 10.2ns$ (s. Signal 5B) and reaches the primary output Z2 at the point in time $t'_{E_c} + \Delta t_{observe} = 11.2ns$ (s. Signal Z2). So this error leads to a failure of the adder circuit.

The second crosstalk error stimulated by $(S)_2$ at the point in time $t_{trans2} = 20ns$ occurres at the point in time $t'_{E_c} = t_{trans2} + \Delta t_{control} + \Delta t_{ij'} = 20.2ns$ (s. Signal 5B). But in contrast to the first one it is compensated completely at gate 8 due to the OR-combination with the delayed 1-state at the side input B (s. Signal 6B) of gate 8. Hence, $(S)_2$ stimulates an error which doesn't cause a failure of the adder circuit.

TABLE II
Test Sequences $(S) \in \{(S)_{real}\} \subset \{(S)_{ideal}\}$

$(S)_{ideal}$		$(S)_{ideal}$	
$((1,1),(0,0),(0,1))$	$\in \{(S)_{real}\}$	$((0,1),(1,0),(0,1))$	$\in \{(S)_{real}\}$
$((1,1),(0,0),(1,0))$	$\in \{(S)_{real}\}$	$((0,1),(1,0),(1,0))$	$\in \{(S)_{real}\}$
$((1,1),(0,1),(0,1))$	$\in \{(S)_{real}\}$	$((1,0),(0,0),(0,1))$	$\in \{(S)_{real}\}$
$((1,1),(0,1),(1,0))$	$\in \{(S)_{real}\}$	$((1,0),(0,0),(1,0))$	$\in \{(S)_{real}\}$
$((1,1),(1,0),(0,1))$	$\notin \{(S)_{real}\}$	$((1,0),(1,1),(0,1))$	$\notin \{(S)_{real}\}$
$((1,1),(0,1),(0,1))$	$\notin \{(S)_{real}\}$	$((1,0),(1,1),(1,0))$	$\notin \{(S)_{real}\}$
$((0,1),(0,0),(0,1))$	$\in \{(S)_{real}\}$	$((1,0),(0,1),(0,1))$	$\in \{(S)_{real}\}$
$((0,1),(0,0),(1,0))$	$\in \{(S)_{real}\}$	$((1,0),(0,1),(0,1))$	$\in \{(S)_{real}\}$
$((0,1),(1,1),(0,1))$	$\in \{(S)_{real}\}$	$((1,0),(1,0),(0,1))$	$\notin \{(S)_{real}\}$
$((0,1),(1,1),(1,0))$	$\in \{(S)_{real}\}$	$((1,0),(1,0),(1,0))$	$\notin \{(S)_{real}\}$
$((0,1),(0,1),(0,1))$	$\in \{(S)_{real}\}$	$((0,0),(x,x),(0,1))$	$\in \{(S)_{real}\}$
$((0,1),(0,1),(1,0))$	$\in \{(S)_{real}\}$	$((0,0),(x,x),(1,0))$	$\in \{(S)_{real}\}$

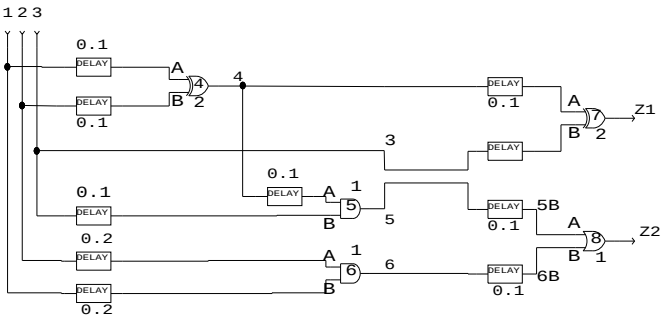

Fig. 4. 3-Bit-Adder

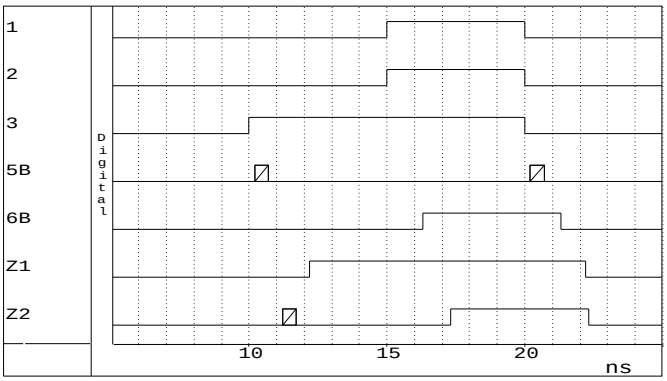

Fig. 5. Propagated resp. Compensated Crosstalk Errors

V. Summary and Conclusions

An improved approach for the logic modeling of reflection and crosstalk errors has been presented. These errors are modeled by uncertain logic states lasting for the duration of an error. Furthermore, it has been shown that stimulation, propagation and compensation of reflection, and crosstalk errors are highly influenced by gate and transmission line delays. Therefore these delays have to be taken into account within test procedures. The presented test generation algorithm is the first published approach taking the error durations as well as the gate and transmission line delays into account.

Acknowledgements

This work is supported by the German Government, Department of Education, Science, Research and Technology (BMBF), under grant 13MV0206. The responsibility for this publication is held by the author only.

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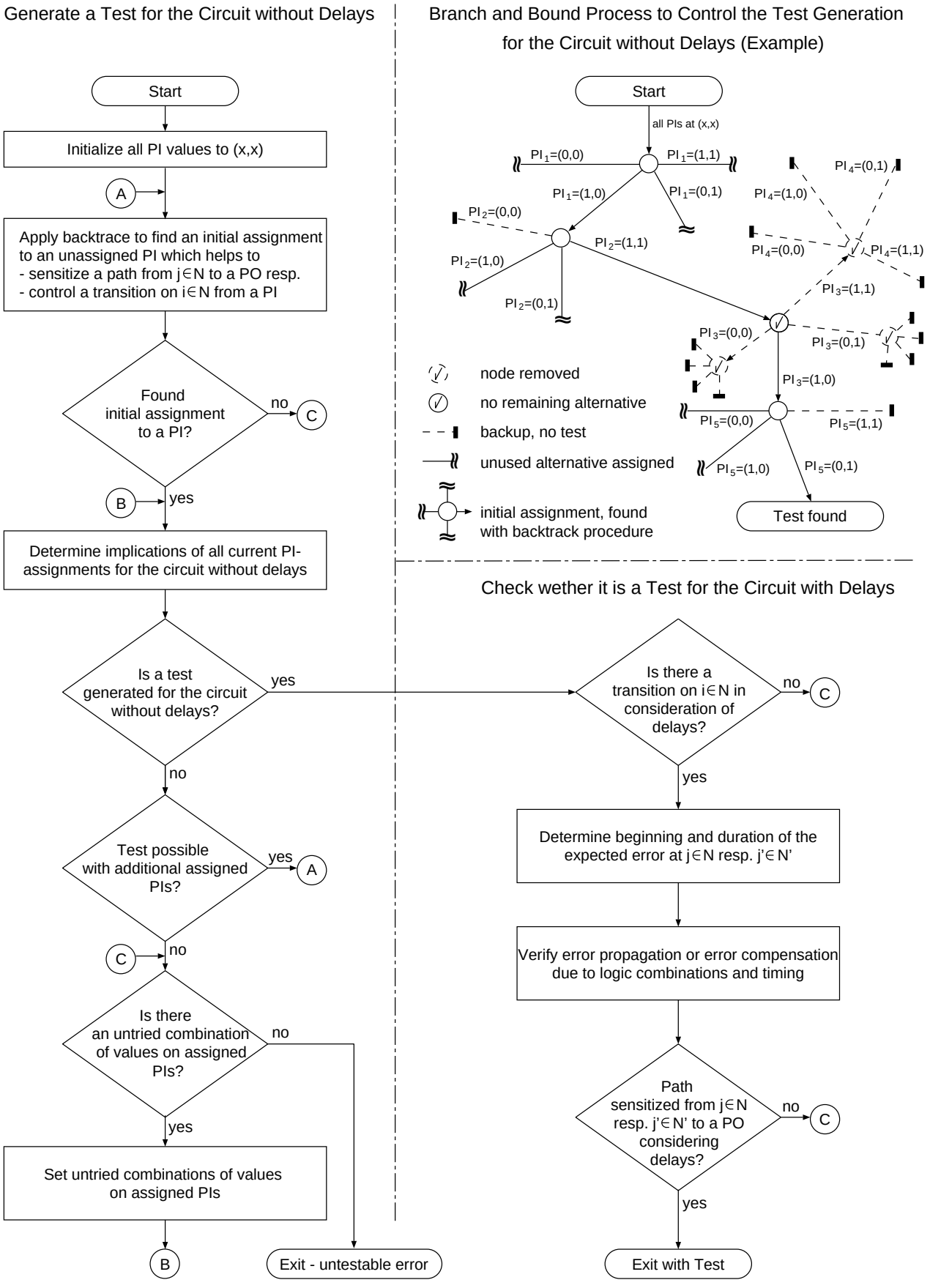

Fig. 3. Test Generation Algorithm (PI = Primary Input, PO = Primary Output)