Choosing a Digital Simulator

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Abstract - This paper summarises the second in a series of benchmarking efforts conducted by DA Solutions between August 1995 and April 1996, for VHDL and Verilog simulators.

The paper discusses the methodology used and the results of an independent public benchmark for leading VHDL and Verilog simulators, for RTL, Gate, VITAL and Co-simulations products. The paper also makes performance comparisons between VHDL and Verilog technologies and between PC and UNIX solutions.

I. INTRODUCTION

A. Background

Simulation technology continues to evolve forcing an aggressive, but welcome development of faster and faster simulators. System and ASIC designers are the winners, but the problem of choosing "which simulator is best for my job" is getting more and more difficult and the cost of evaluating huge numbers of simulators in the market becomes prohibitive. Relying on vendors' information can be both misleading and often costly.

Benchmarking has always been a difficult and frustrating task. Making real "apples to apples" comparisons is difficult. Running "real world" designs is equally arduous. The tendency is to reduce the results into a table or graph, which tells only one part of the story.

DA Solutions has developed an approach for benchmarking simulators [1]. We have taken a pragmatic approach to building a benchmark suite from user-supplied designs and have developed good working relationships with consumers and vendors to ensure each product gets a fair presentation. One essential element for a good benchmark is to remain independent and show a desire for fairness.

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B. Objectives

Our objectives for conducting the benchmarking exercises were numerous but most importantly:-

1. to place in the public domain independent and unbiased measures of simulation performance;
2. to provide CAD vendors with competitive data;
3. to create a maintainable industry standard benchmark library.

C. Criteria for a Good Benchmark

In order for an independent benchmarking system to gain the confidence of both vendors and users of simulation products it must:-

a) mirror the real world of evaluation of tools by users;
b) use a benchmark library that is representative of a wide range of user applications.

D. Benefits

Because this benchmarking effort is done periodically [2],[3],[4] vendors have realised some important benefits. Each time they participate in the benchmarking exercise, they learn more about their products and strive to improve it in order to remain competitive.

The electronics designers are the real winners. They get solid, unbiased information about all leading simulation products. The information contained in the report [4] can be used as an important part of the information gathering process. The use of the report as a first level of the decision process has been known to reduce the cost on internal benchmarking efforts by as much as 30%.

In addition, because each company continues to improve their products based on information gained in the benchmarking process, their customers get a better product.

II. Benchmarking Methodology

DA Solutions used an approach described in more detail in [1], [2] that satisfied both vendors and users. Two years ago DA Solutions set-up a "Benchmarking Group" consisting of users and vendors to define set of benchmarks, the methodology and themeasurement criteria for evaluating VHDL and Verilog simulators. This partnership was the key in the success of this benchmarking exercise.

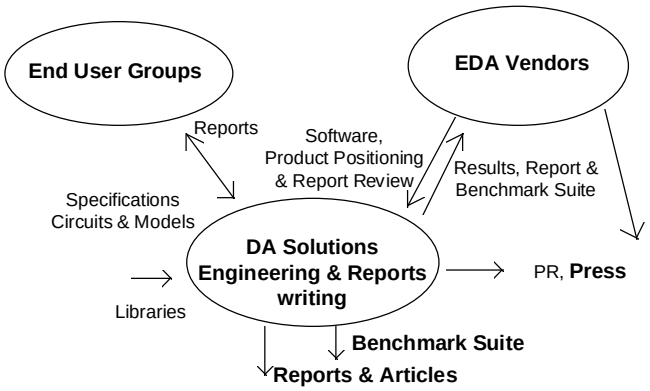

Fig. 1. Relationship Between The Benchmarking Groups

DA Solutions worked with EDA Vendors, Tool Users and Silicon Houses to establish a series of benchmarks that reflect the differentstyles and applications of ASIC designs. We ran these circuits through different VHDL and Verilog simulators. The purpose was to measure the functionality, performance and limits of each simulator when used as part of the ASIC design flow. We established a large and growing library of 'real' designs that represents a wide range of applications reflecting different styles and technologies. Each circuit is supported with its own testbench and theexpected simulation output for verifying the correctness of the results.

We ran the benchmarks on our workstation and PC in the same manner as the real world user would, using each simulator in the optimum vendor recommended way to achieve the best overall performance. Each vendor validated the results of their own simulator, using the same benchmark library to ensure the accuracy of the results prior to publication of the results.

We produced a report tabulating product functionality, source editing capabilities, compilation, elaboration and execution times together with the peak memory required during simulation. The report further catalogues product features, platforms, libraries, linkage to other EDA tools, pricing and availability.

We conducted comparisons between VHDL and Verilog and between products run on Workstation/UNIX and PC/NT using benchmarks common to languages and to platforms.

We evaluated several types of simulators: C code compiled, native code compiled, interpreted and cycle based. The exercise covered: VHDL at RTL, gate, mixed and VITAL and Verilog at RTL, gate with SDF and PLI.

III. Participating Vendors And Products

Invitations were sent to a large number of small and large companies that specialise in VHDL or Verilog simulators. Table I lists the companies that participated in the 1995/6 program, their products and the technology tested.

TABLE I

Benchmark Participants : Vendors & Products

EDA Vendor	Products	Language	Technology
Cadence	Leapfrog 2.2	VHDL, VITAL & SDF	Native Code Compiled
		VHDL/Verilog Co-Sim	Native Code Compiled
Fintronic	FinSim-ECS 4.3	Verilog PLI & SDF	C++ Code Compiled & Interpreted, Cycle Based
IKOS	Voyager VS 2.2	VHDL / RTL & Gate	C Code Compiled
	Voyager CS 2.2	VHDL Gate	C Code Compiled
	Voyager NSIM	VHDL Gate	C Code Compiled
Mentor	QuickHDL 4.5a	VHDL, VITAL & SDF	Native Code Compiled
		Verilog & SDF	Native Code Compiled
		VHDL/Verilog Co-sim	Co-Simulation
Synopsys	VSS 3.4b6	VHDL ,VITAL & SDF	C Code Compiled & Interpreted
VEDA	Vulcan 3.0	VHDL, VITAL & SDF	Compiled & Interpreted
VeriBest	4.2.0.1 PC	Verilog, PLI & SDF	C++ Code Compiled & Interpreted
ViewLogic **	Optium V5.4	VHDL, VITAL	C Code Compiled
	SpeedWave MT 5.3	VHDL, VITAL	Multi Thread
	Fusion 1.2	VHDL & Verilog	C Code Compiled & Native
	VCS 3.0B1.1	Verilog, PLI & SDF	C & Native Code

** ViewLogic withdrew from the benchmark.

IV. The Benchmark Library

Eighteen different 'real' ASIC designs were acquired from leading systems and silicon houses . A number of these designs are modelled at different levels of abstraction thus producing a total of 44 variants comprising the benchmark library. Fourteen circuits were modelled in VHDL, nine were modelled in Verilog, three were used for the co-simulation test and four VHDL designs tested with VITAL

libraries and SDF back annotation files. We have also developed Linear Feedback Shift Register (LFSR) circuit of varying sizes between 50K and 3,200K gates used for capacity tests. The benchmark library represented a wide range of applications:-

4 Processor designs; 3 telecommunications; 2 networking; 1 signal processing; 2 aerospace; 1 audio / video decoder; 1 arithmetic; 2 core models; 8 capacity test.

The design sizes varied between 1000-21000 lines of code representing circuit sizes between 40 Kgates and 32,000 Kgates.

V. Results Summary

In this section we present our general observations of the benchmark results. Later sections will highlight the main features and strength of the individual company and their products.

- Product quality in general was not as high as it was in the previous year. We witnessed a slight degradation in quality across most products at the expense of performance. This was mainly relating to software bugs and conformance to the standards. On average we evaluated four releases from each vendor. One vendor delivered twelve releases in total.

- Inter-operability Issues - in addition to software corrections, a significant amount of reworking of models (but without changing the functionality) was necessary in order that they executed successfully in all the simulators.

- We have witnessed a significant improvement in performance over the past three benchmarking exercises, and with each successive product release during each exercise.

- The most prominent new features of the benchmarking exercise are the inclusion of VITAL simulation, Co-simulation and products running on PC.

- The number of products supporting VITAL is growing rapidly, but most of them are still in infancy suffering from problems of interpretation of VITAL as the standard moved from release 2.2b to the official 1076.3 (VITAL 93). This led to problems with inter-operability of benchmarks across the products. The majority of the products (apart from one or two) are still suffering from poor performance, acceleration is rapidly being engineered producing faster run time with every release.

- The number of products supporting Co-simulation of VHDL & Verilog is also growing fast, that is in spite of the growing number of products supporting VITAL. This leads us to the belief that availability of ASIC Libraries is not the only factor for using co-simulation, but as the two standards are becoming equally used, the re-usability of code is a dominant factor. There are several approaches to co-simulation, the most flexible is that provided by Mentor Graphics "QuickHDL", but only the methodology common to all products was used for this exercise.

- Very soon, the PC will be playing a major role in supporting Design Automation Applications. The Pentium Pro 200, used during the exercise outperformed those products running on workstations & Unix. The cost performance ratio between PC/NT and UNIX systems of equal processor speed can be as much as 10x.

- At the RTL level, the performance gap between VHDL and Verilog products running under UNIX is rapidly closing "Fig. 2&3". However, the gap is wider for those products specifically using PC and cycle based simulation.

- No single VHDL product achieved an overall leadership position.

    - Mentor Graphics QuickHDL maintained its leadership to be the fastest in analysis and compilation.
    - Cadence Leapfrog and VEDA's Vulcan dominated the VITAL Group.
    - Of the mixed level simulators evaluated, IKOS-CS & NSIM provided the fastest execution performance.
    - Synopsys continue to improve their product performance with every release. VSS is a serious competitor in VHDL simulation "Fig. 2.".

- Fintronic (USA) dominated the Verilog group.

- When comparing VHDL with Verilog, Fintronic (USA) contributed to the Verilog success in widening the Verilog / VHDL performance gap.

- Mentor Graphic's QuickHDL is the most flexible and versatile product available; three products in one; its support for VHDL alone, Verilog alone or in Co-simulation, in one kernel makes it the most versatile product on the market.
- Multi threading did not achieve the performance gain witnessed in the 1994/95 exercise. Increasing the

number of threads/processes did not seem to make much impact.

- Circuit application, coding style and simulation technology, continue to be major factors with regard to performance.

- Within the computer configuration used, 800K gates remains the maximum capacity achieved with full timing libraries.

The full Report [4] presents the hard facts in far more detail than can be included here. In addition to providing feature and pricing information, approximately 50 tables of data provide comparative information, for each tool. We measured the compilation, elaboration (or loading) simulation times, we also recorded the total execution times and memory utilisation for the following :

- VHDL RTL and Verilog RTL designs,
- VHDL mixed and gate level and Verilog designs
- VHDL with VITAL designs
- VHDL & Verilog Co-simulation designs
- Comparison between VHDL & Verilog
- Capacity test for VHDL & Verilog at the gate level

VI. How Did Each Vendor/Tool Perform?

The bar charts "Fig. 2 & 3" provide a mere glimpse of some of the tests that have been conducted, namely that of the simulation performance for VHDL and Verilog at the RTL level. The full report contain other charts and spreadsheets for all categories of tests. A summary of the salient facts for each vendor is presented in the list below by company name in alphabetical order:

A. Cadence Design Systems

Leapfrog 2.2, a native code compiled VHDL simulator, was the only Cadence product placed in the benchmarking exercise. Leapfrog has consistently occupied a prominent position in the benchmark for all categories.

The Leapfrog VHDL Simulator has exhibited fast simulation performance across the majority of the designs. We believe this is due to the native-compiled code approach. The native compiled code approach provides better performance for all types of VHDL descriptions spanning from behavioural/RTL to gate-level designs.

For the RTL compilation, it consistently occupied second position to Mentor Graphics, but in simulation it occupied four firsts and five seconds. However Laepfrog is not as efficient as QuickHDL in the RTL memory utilisation.

Leapfrog's VITAL implementation has dominated this group with three firsts and one second, both when reporting simulation and total execution times.

With Co-simulation, the measured compilation time is for the VHDL test bench only, as the Verilog source is interpreted during execution. Leapfrog again showed very good performance speed as a result of the "tight coupling" of Leapfrog with Verilog -XL.

At the Gate level, it was not as successful, particularly in the presence of IKOS Voyager CS and NSIM.

At VHDL capacity, it averaged 120 bytes per gate beating Voyager CS into second place.

B. Fintronic (USA)

FinSim4.2.0.1 is C++ code compiled and interpreted Verilog simulator. Finsim-ECS 4.3 is an enhanced cycle simulation (ECS) delivered in the second part of the evaluation exercise, consisting of the simulator FinSim and the ECS engine. FinSim-ECS automatically identifies the parts of the circuit that are suitable for simulation on the ECS engine and the rest is simulated by FinSim. Changes between FinSim 4.2.0.1 and FinSim-ECS4.3 has shown speedups on certain benchmarks between 8 and 12 times particularly for designs that seem to suit the ECS paradigm. FinSim displayed the best overall simulation runtime of the Verilog products on the SPARC 10/40.

FinSim was one of the simulators tested on the PC Pentium Pro 200. The performance of Finsim on the PC has not only surpassed all verilog simulators on UNIX, but has succeeded to out-perform all other simulators (VHDL and Verilog). This lead us to believe the PC will play a major role in the EDA industry.

In capacity tests, FinSim achieved 200k gate within the 64Mbytes memory, averaging 223 bytes per gate.

C. IKOS Systems Inc.

Voyager VS 2.2, a VHDL simulator, Voyager CS 2.2, accelerated gate level, proprietary language simulator with VHDL interface, and NSIM, a hardware accelerator. Of the mixed level simulators, IKOS delivered the best execution performance with both unit delay and fully timed libraries. IKOS achieved the highest performance with circuits that were heavily dominated by event activity.

On average Voyager VS performed adequately at the RTL level. Its main draw back has been in the analysis and compilation phase using Compass' VTIP. Its memory utilisation is good and occupied many second positions.

At the gate level, with Voyager CS and NSIM, the compilation run times improved marginally. NSIM performed better than all other products at simulation time for those benchmarks where libraries were available.

IKOS does not at present have VITAL solutions. We did not evaluate Omega (accelerated Verilog simulator) nor did we benchmark any co-simulation product if the latter exists.

D. Mentor Graphics Corporation.

QuickHDL, a native code compiled simulator gradually replacing QuickVHDL and QuickSim. QuickHDL is the most versatile product we have benchmarked in that it is a VHDL, a Verilog and a mixed VHDL/Verilog simulator all in one kernel.

QuickHDL delivered the fastest compilation speed for the whole of VHDL and Verilog benchmarks running on the Sparcstation. When measuring the simulation performance alone at VHDL/RTL, "Fig. 2", QuickHDL shared the leading position with Cadence and Synopsys. But the position improved considerably when including the set-up time (i.e. analysis, compilation and elaboration) as part of the full execution time. This is particularly due to the superior compilation speeds. QuickHDL demonstrated the best overall memory utilisation.

For the capacity test QuickHDL, running VHDL only, reached 400K gates within the available memory. It averaged 170 bytes per gate.

The Verilog offering is continually improving with every successive release, and will soon become a competing stand-alone product..

In the Co-simulation mode it offers the best product in flexibility, in that the VHDL and Verilog can be mixed in any combination of hierarchy, without resorting to elaborate interface definition. For instance, a VHDL module can instantiate a Verilog which in turns, instantiates VHDL and so on. Full exploitation of this feature was not tested. The applied test was concentrated on using VHDL testbench with Verilog netlist which was common to all other co-simulation products.

E. Synopsys Inc.

VSS3.4b6 has two modes of simulation; C code compiled and interpretative, a useful facility when selecting the appropriate mode to suit the different design phases. We concentrated our benchmarking on the C code compiled option.

VSS is the fastest developing simulator, it continues to improve in performance delivering highly competitive execution times at the RTL level when compared with other simulators. VSS has consistently shown performance gains between x1.5 and x8 over last years release VSS3.1b, across the whole of the RTL set. VSS scored 3 firsts and 5 seconds the other 4 were very close in third place. Synopsys achieved best performance with circuits that called for heavy arithmetic manipulation. The drawbacks with VSS is during the analysis and compilation phase, impacting the total execution time.

VSS demonstrated good memory utilisation in the RTL group. For the capacity test VSS achieved 400K gates, equal to other products in the group. This is x4 improvement over last year's performance. The average bytes per gate is 165.

Synopsys' enthusiasm in supporting this benchmarking exercise is unrivalled. We are indebted to Synopsys in converting VITAL libraries from 2.2b to 3.0 libraries using library compilation part of the synthesis tools.

F. VEDA Design Automation Limited

Vulcan 3.0 is a single kernel VHDL simulator supporting both RTL and gate level. The interpreted or compiled mode is selected automatically at run time depending on the circuit structure. VITAL acceleration is the main feature of this product. Vulcan has consistently demonstrated leadership in this group. They achieved 3 firsts and 1 second during the exercise only to be overtaken by Cadence in the last few days of the exercise. Presently their position is a very close second to Cadence. VEDA, is working to improve the performance of the RTL simulation. We will be witnessing major speed-ups in the not too distant future.

The memory utilisation for VHDL RTL is reasonable, having attained three seconds. Similar memory performance has been seen for the VITAL tests. During capacity tests, Vulcan achieved 200k Gates averaging 326 bytes per gate.

G. VeriBest, Inc.

VeriBest Verilog simulator is an OEM from Fintronic (USA). It is available on the Intergraph TD range of personal computers running Windows NT. VeriBest simulator interfaces with many other CAD tools supported on the PC, making it the best low cost design solution available. As reported VeriBest is the best overall Verilog simulator and has managed to beat other VHDL simulators

using common circuits described both in VHDL and Verilog. VeriBest contains FinSim release 4.2.0.1

VII. Summary- which Simulator?

The 1995/96 benchmarking exercise was a success. Interestingly it showed that no single tool vendor won on all tests. It also demonstrated that, contrary to previous belief, VHDL solutions are quickly catching up with the Verilog offerings and in certain cases has equalled in performance. The exercise also demonstrates that simulation performance is a complex parameter depending on combination of coding style, simulator technology, and hardware platform and computer configuration (processor speed, memory, disc space and disk access time). The exercise has also confirmed our belief that the PC will be playing a major role in the EDA industry very soon. A report [4] is published supplied with the benchmark library.

In conclusion, our recommendations appear in Table III.

TABLE III
Choosing A Digital Simulator

For Application	Choose
VHDL RTL	Leapfrog, QuickHDL or VSS
VHDL & VITAL	Leapfrog or Vulcan
VHDL accelerated gate	Voyager CS and/or NSIM
VHDL/Verilog Co-sim	QuickHDL or Leapfrog
Verilog RTL	FinSim ECS
Verilog Gate	FinSim ECS
Verilog on PC	FimSim or VeriBest

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The exercise has been - and continues to be - well supported by the EDA vendors through funding and the supply of products for evaluation. We acknowledges the high amount of support and motivation that has been provided by the vendors for the establishment of these benchmarks.

We also acknowledge the help of SUN Microsystems and Intergraph Electronics for the loan of computers for the multi threading tests and PC tests.

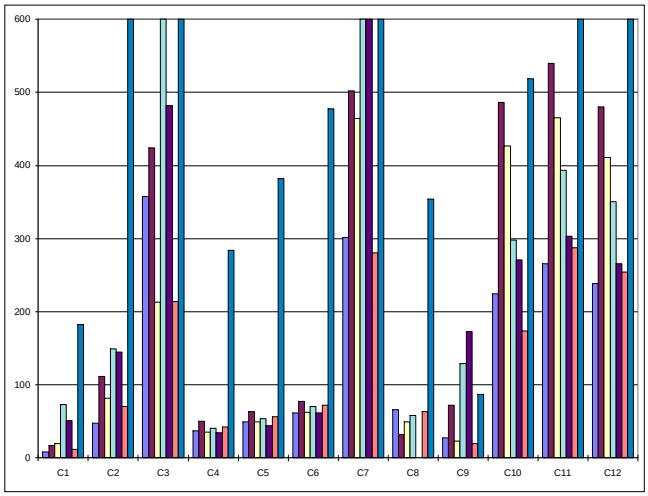

Fig. 2. Simulation Times in CPU Seconds for VHDL / RTL

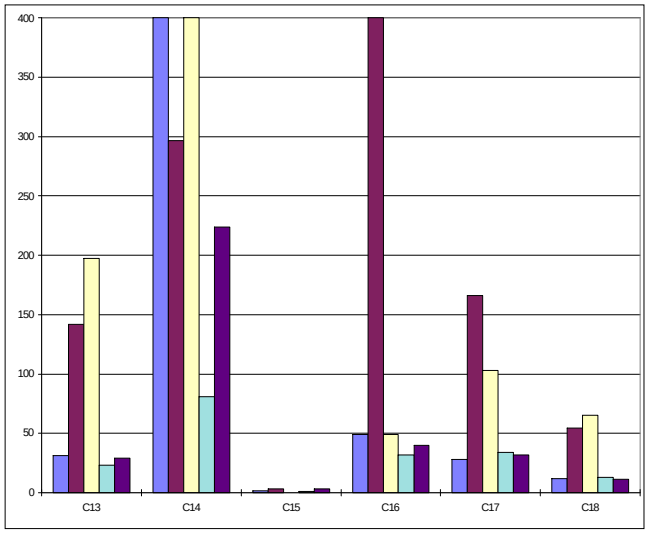

Fig. 3. Simulation Times in CPU Seconds for Verilog/RTL

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