VLSI Design and Education Center (VDEC) Current status and future plan

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Abstract - After briefly reviewing a history of VDEC, its functions and facilities are summarized, followed by future plans of chip implementation along with a network society.

1. INTRODUCTION

Just after the MOSIS in U. S. A (MOS Implementation System) started in early 80's, the first study in Japan was done by a research group led by Prof. T. Sugano, to establish a nation-wide organization for supporting implementation of VLSI chips designed in universities. Major universities as well as many semiconductor companies joined this activity for studying a possible Japanese system and published a proposal[1].

According to the proposal the final system would be established in some steps and organized as a distributed network system. Here, two major centers are placed in the east and west regions of Japan, to which several local satellite centers are connected. User universities are connected to the nearest local satellites.

Although this activity and the proposal were stimulated by the MOSIS activity, it paid an attention not only to chip implementation support but also to basic research promotion in the field of VLSI fabrication technologies in Japan. In this sense it was a pioneer work for establishing a COE in the field of VLSI technologies.

The above proposal was, unfortunately, not realized for some reasons. So, it is a great pleasure for us to see the realization of the VLSI design and education center, VDEC, though the system is a little changed from the original plan. In this paper we describe the outline of VDEC, established in May 1996, and its future plans.

2. PURPOSE AND ORGANIZATION

VDEC is an inter-university center placed in the University of Tokyo, which has a mission to continuously promote and support VLSI education programs in Japanese universities, including the nationals and the privates. The center organization, in terms of center staffs, will be brought to completion in two years, 1996 and 1997, which consists of a research

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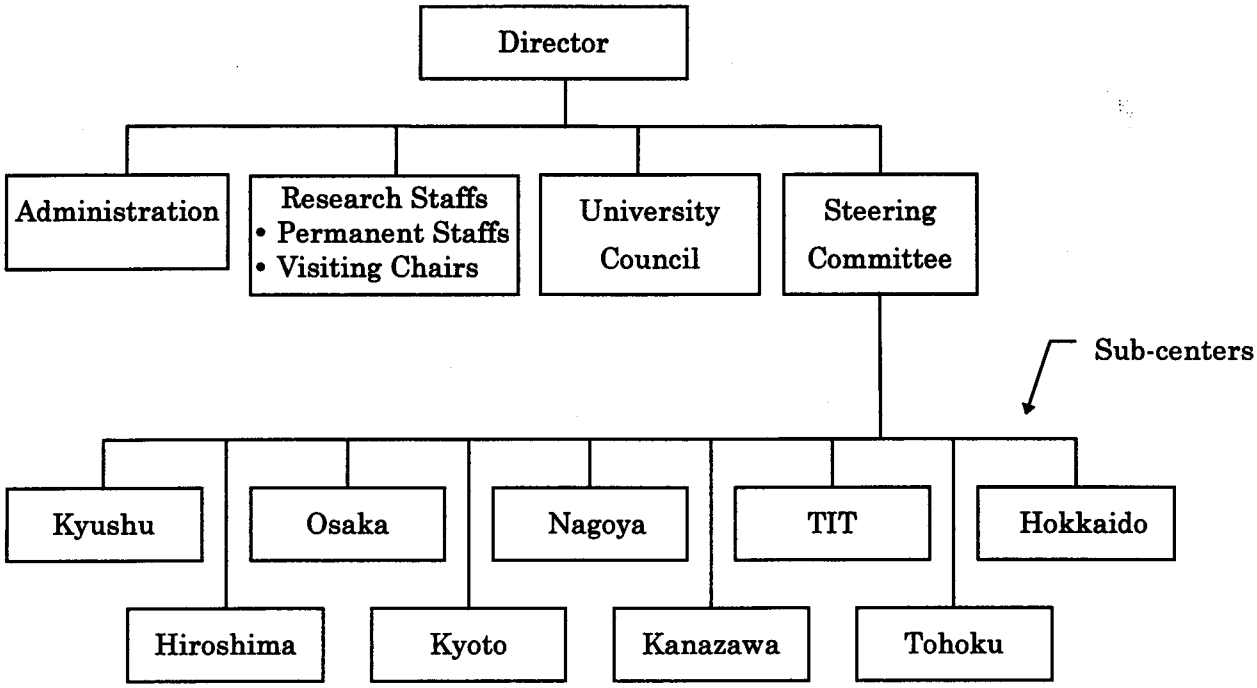

Fig. 1 Organization

division and an administration division.

The research division includes VLSI design field and CAD field, and staffs in the both fields collaborate to fulfill the above mentioned mission. The center activities are governed by an steering committee, members of which are representatives of the national and private universities in Japan.

In 1997, we have a plan to invite a visiting professor from industries. Two chairs for visiting associate professors from other universities are also planned in 1997. These visiting chairs are used for inviting professionals for 2 or 3 years, for the purpose of promoting collaborations with semiconductor industries and inter-university activities. The total number of the center staffs, including the administration division, is expected to be about 12.

3. FACILITIES

VDEC will provide several facilities for users in all the Japanese universities. The facilities are categorized into hardware and software.

The hardware facilities have been already introduced last year in advance in VDEC as well as in 9 major universities, that we call *sub-centers* hereafter. These sub-centers corresponds to the satellite centers in the Sugano plan mentioned above. Although these sub-centers are currently not yet established as the official organizations in terms of dedicated staffs, we are expecting that these universities will organize the official sub-centers with permanent staffs in near future, with individually unique features in VLSI education for realizing a nationwide network center system tightly collaborating with VDEC.

The VDEC hardware facilities consist of

test facilities and *mask facilities*. The test facilities include

(1) a digital tester with a mixed signal option,
(2) an analog parameter analyzer,
(3) an electron beam probe for measuring electric potential on chip, and
(4) a focused ion beam machine to modify chip interconnections.

A low temperature and a high temperature probes are also provided for special testing.

On the other hand, the mask facilities are composed of an electron beam machine for mask delineation and development/etching systems. These facilities will be used for making masks for multi-project chips efficiently and inexpensively for cases of relatively conservative full custom design rules. These facilities are expected effective especially to fabricate full custom chips with small volumes, due to the fact that the major part of fabrication cost is occupied by the mask preparation in these cases. The operation of the facilities will be supported by makers of the electron beam machines and masks.

As for the software facilities, the CAD software for VLSI designs are purchased based on yearly rental contracts, under the condition that the software can be used all over the universities in Japan for the purpose of education and researches. The yearly rental method was chosen so as to always provide the newest CAD software, which are continuously renewed year by year.

The CAD software covers almost all design fields, from the high level design by HDL and synthesizer to the physical level design by the graphic interface. The first target of the CAD software is, of course, to design real chips. An attention is, however, also paid to FPGA mapping. FPGA users will be able to design logic architectures to be programmed into FPGA using these software. Then physical programming of FPGA will be done by FPGA-specific writers, which should be prepared by users themselves.

The rental fee of CAD software is covered by the VDEC budget, so that users can use them with almost free of charge based on yearly registration, though a small amount of handling fee might be charged. Program codes of CAD software will be distributed by CDROM or network and copied into users' local workstations, while the licenses are controlled via the network by the sub-centers as well as VDEC. The registration for the CAD software will start from the next year and be ready for use from the beginning of 1997 April.

4. FUNCTIONS

The first year, 1996, is a preparation term of VDEC for the real start of services in 1997. A practice of *test run* of real chip implementation is under going, collaborating with sub-centers as well as other major universities. The purpose of the test run is to clarify possible problems in the chip implementation and to prepare libraries to be used from 1997.

So far, we have made rental contracts for workstations to be used in seminars, a server computer to be used for a license server and chip design processing, and CAD software.

From 1997 April, we will start chip fabrication services twice a year for each

category of CMOS technologies; 0.5um CMOS (NTT Electronics Technology) full custom design for high speed logic applications, 1.5um CMOS (Motorola Japan) full custom design for general purpose applications including analog, and Laser-programmable gate array, LPGA (SONY/Chip Express), for logic system designs. Although details of the schedule will be settled in the steering committee, we will pay attention so as to synchronize with curricula of VLSI education in universities.

The interfaces between VDEC and users in the chip fabrication services are mainly based on the graphic level format of GDS-II for full custom designs. As for the LPGA, we are now discussing with SONY/Chip Express on the interface; either net-list-level or physical level. In the pilot project sponsored by the Ministry of International Trade and Industry in 1994 and 1995, the design interface for gate array was a net-list-level one. This way of interface may be attractive for users oriented to system designs. But, it is rather expensive due to the processing cost for mapping net-lists to layouts along with back-annotation. In order to establish an inexpensive way to fabricate real chips, it would be indispensable for universities to have a skill to prepare their designs in a physical level. This may be bothering for system designers. We are planning seminars for CAD tools and VLSI design methods, and expecting to form a network collaboration system to help each others to cope with this kind of bothering problems. The network collaboration system did work in the test run this year. It was more than our expectation. Researchers and students could effectively communicate via network for exchanging technical information about design. From this experience, we are convinced that a *network society* of VLSI designers in universities will be formed as a natural consequence of VDEC functions to share the common design knowledge and store design resources.

The chip fabrication cost is basically charge to users depending on chip area. It will be, however, much cheaper than MOSIS and Eurochip owing to the VDEC facilities mentioned above, as well as the semiconductor companies and a mask making company (Dai Nippon Printing). As for the details on the chip prices, please refer to *www.vdec.u-tokyo.ac.jp*. We would like to express sincere thanks to these companies.

5. FUTURE PLAN

As mentioned above, VDEC will practically start services from 1997 fiscal year. We think, however, that CAD tools and chip fabrication services are not enough for promoting VLSI design education, but just a beginning. We have to prepare/revise new curricula matched with CAD tools and real chip designs. We also have to introduce basic test facilities to all the universities interested in VLSI design. Further collaboration will be indispensable for realizing the nation-wide VLSI design education.

On the other hand, interchange of technical information as well as specialists between universities and semiconductor companies is another key issue for promoting

VLSI design education. Historically many advanced design concepts and know-how have been produced in semiconductor companies. The visiting chair for a specialist from industry is expected to play a key roll to this end.

There are several organization in the world, which have a similar mission such as MOSIS, Eurochip, CIC in Taiwan, IDEC in Korea and so on. In future we hope to promote international collaborations in VLSI design education, too.

[1] T. Sugano et al, "Proposal: Distributed Inter-University Research Organization for Education of Integrated Electronics ," IEEJ Report, 1985 April

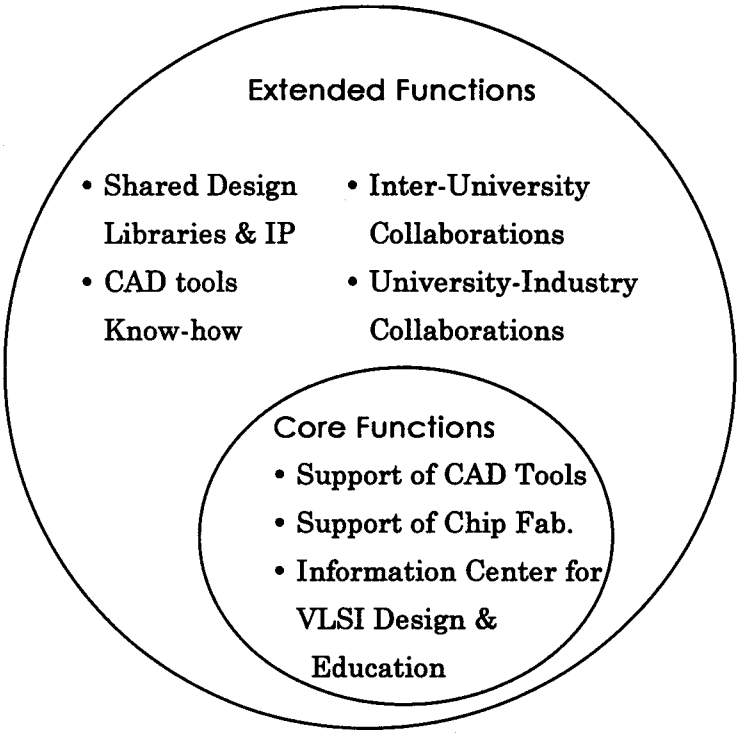

Fig. 2 VDEC as a core of VLSI education