Multi-Project Chip Service for University and Industry in Taiwan

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Abstract - Acting as the bridge between the designers and manufacturing companies, Chip Implementation Center (CIC), founded in 1992 under National Science Council, aims at the services for the fabrication of multi-project chip, the procurement / integration of software CAD tools, and the promotion of IC design / testing / CAD software technology.

To date, 2000 academic licenses of software CAD tools have been obtained and 739 chips of the academics have been fabricated through CIC.

I. INTRODUCTION

The integrated circuit has long been called the rice of electronic industry which is generally regarded as a key strategic industry. Also, it has much bearing on some crucial hi-tech industries such as those of communication, information, computer, etc. Since 1991, the integrated circuit has remained on the top of all the imports of the Republic of China. In view of this, National Science Council (NSC) in 1992 initiated a long term plan - Chip Implementation Center Special Project - in preparation for a National Chip /SYSTEM Implementation Center. National Science Council invited the well-experienced experts from the academic, industry, and research organization, to form a Steering Board. Strategic advice and overall supervision are the responsibility of the Steering Board.

The missions of Chip Implementation Center are to cultivate well-qualified IC/SYSTEM personnel. Three main activities of CIC are :

- Assist the universities and polytechnics to perfect their design environment.
- Provide easy-of-access and fast-turnaround chip fabrication/measurement service.
- Promote the design technologies of IC/SYSTEM.

Located in the Hsinchu Science-Based Industrial Park, CIC was originally aimed at serving the universities and polytechnics, but recently some of the services have been expanded to the research institutions and related industrial sectors.

In this paper, the multi-project chip (MPC) service for university and industry in Taiwan would be presented. The services in perfecting IC design environment of the academics will be introduced in Section II. In section III, the detail of multi-project chip service is given. The activities in technology promotion are detailed in section IV. Finally, conclusions and future works are given.

II PERFECTING IC DESIGN ENVIRONMENT OF THE ACADEMICS

Following the advice of the Steering Board, CIC selects the popular software CAD tools and integrates them into a complete design environment (as shown in Fig. 1), which covers :

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- full-custom IC design flow,
- cell-based IC design flow, and
- FPGA design flow.

To assist the universities and polytechnics to perfect their IC design environments, the procurement of the academic licenses of those software CAD tools is the responsibility of CIC. The professor can get the licenses of those tools on a pay basis (US$150~400) through CIC. So far, the design environments of 30 universities and 25 polytechnics in Taiwan have been set up and 2000 academic licenses of software CAD tools have been obtained through CIC, as listed in Table I. CIC acts as the consultant for the use of software CAD tools.

III. Multi-Project-Chip Service

The multi-project service of CIC is to merge the designs from the academics, industries, and research organizations, into one set of photo-mask, as shown in Fig. 2.

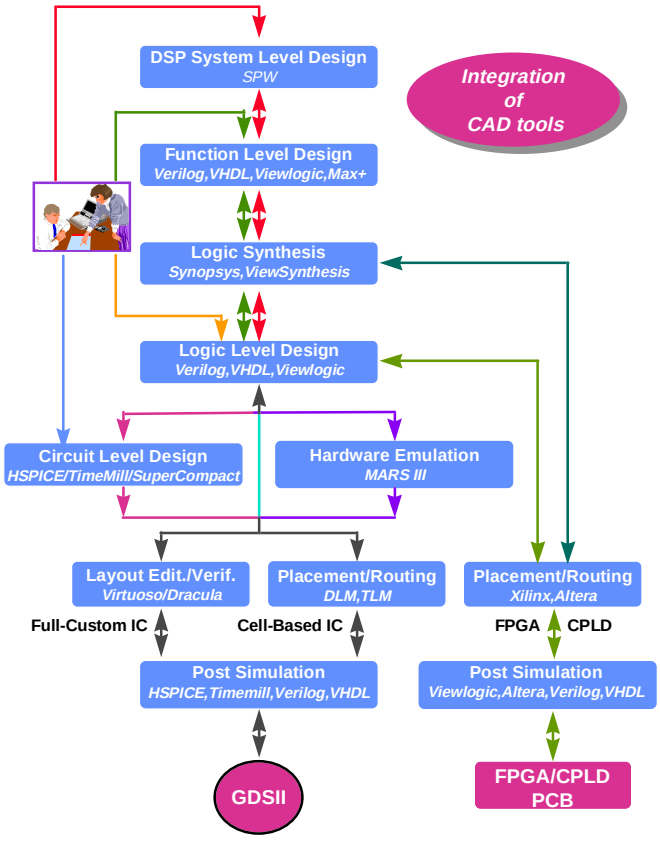

Fig. 1. Integration of software CAD tools

TABLE I
NO. OF SOFTWARE CAD TOOLS ORDERED THROUGH CIC

Software package		No of package
CADENCE	/OPUS(verilog/Virtuso/DLM)	530
	/DRACULA	153
	/ALLEGRO	75
	/SPW	123
Metasoftware/HSPICE		361
SYNOPSYS		139
XILINX (PC+WS)		249+59
ALTERA (PC+WS)		377+97

Fig. 3 shows the roadmap of IC fabrication processes through CIC. Three processes are provided from domestic manufacturing corporations:

- 0.6um SPDM CMOS technology (TSMC)
- 0.5um DPDM CMOS technology (UMC)
- 1.0um GaAs technology (Hexawave)

Three foreign fabrication processes, advised by Steering Board, are also provided :

- 0.8um DPDM BiCMOS technology(French/CMP)
- 0.2um DPDM CMOS technology(French/CMP)
- 2.0um DPDM CMOS technology(Belgium/IMEC)

The command files (DRC/ERC/LVS) of those IC technologies are provided by CIC to assist the designers verifying their designs. After the designed chip passes through the layout verification of those command files, it can be submitted to CIC seeking the opportunity for free-of-charge fabrica

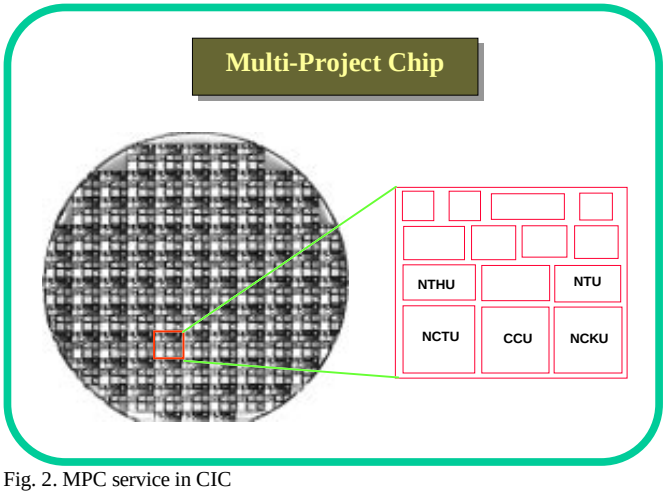

Fig. 2. MPC service in CIC

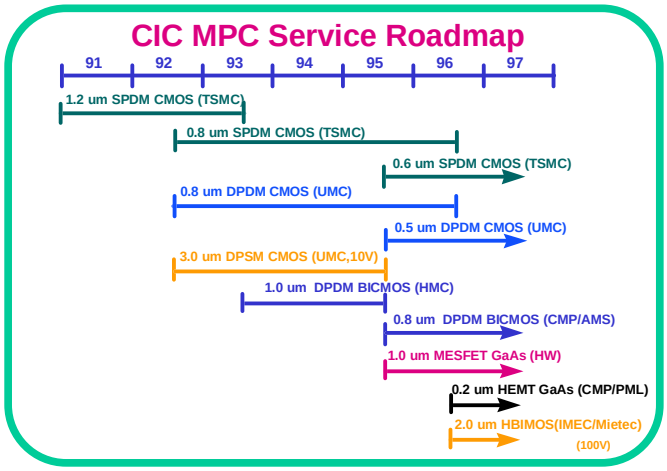

Fig. 3. Roadmap of CIC MPC service

tion. With the recommendations of the Review Board, which is constituted by many well-experienced IC exporters, the designed chip is merged into the multi-project chip, as shown in Fig. 4.

Two types of free-of-charge access to chip fabrication have been identified : educational chip and advanced chip. The

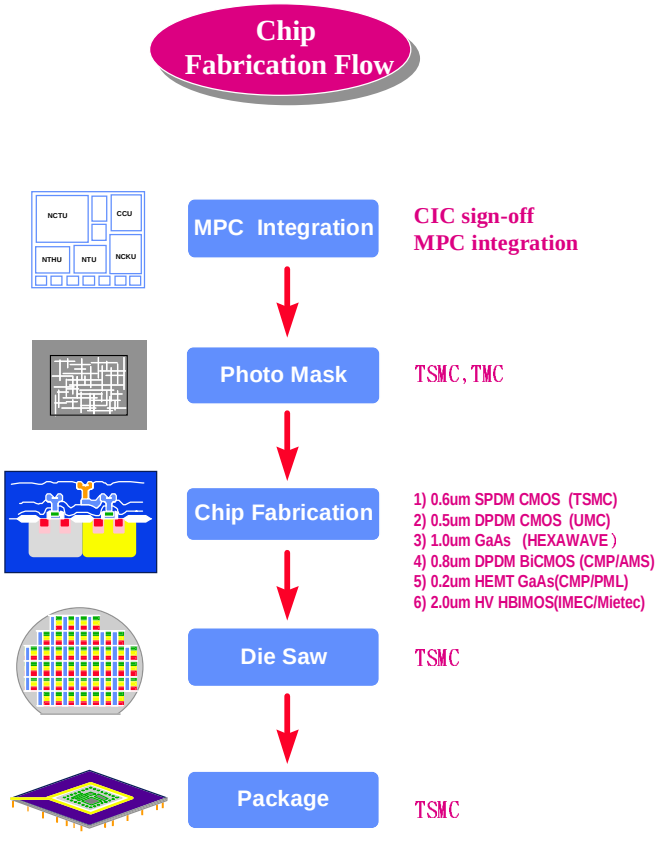

Fig. 4. The fabrication flow of CIC

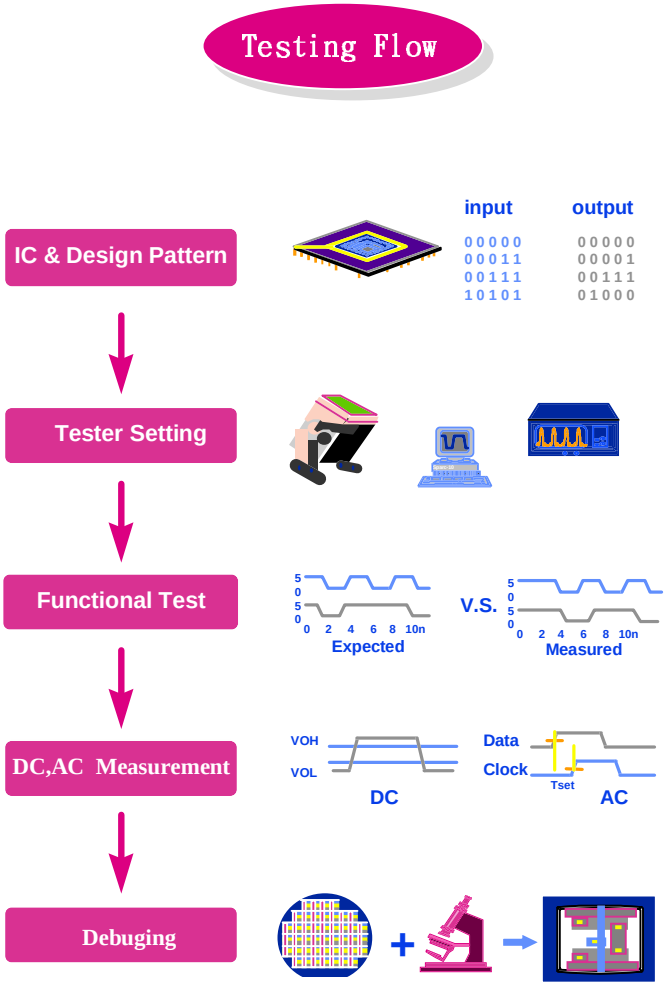

Fig. 5. IC testing environment.

educational chip is a fixed chip area ($1800^2 um^2$) with fixed I/O pin count (28pin) and package (DIP), which is suitable for the experiment of VLSI courses. The advanced chip is research-orientation one and is more flexible in chip area, I/O pin count, and package. The professors, who carry out the project of National Science Council, can apply free-of-charge access to the fabrication of advanced chip.

To help the academics to verify their chip, CIC also set up a IC testing environment (as shown in Fig. 5) for analog/digital IC testing and debugging. To date, the function of the testing environment are summarized as follows:

- Allowed Pin Count : 224,
- Clock Rate : 200 MHz.
- Auto-test pattern translator

- 16 bit ADC/DAC

Industries and research organizations can also access the MPC service of CIC by payment, which is the price = (the price per mm^2) * (area of the design). In general, (the price per mm^2) is NT$7000/$mm^2$ for CMOS and NT$50000/$mm^2$ for GaAs.

To date, 739 prototyping ICs designed by the academics, and 74 by the research institutions as well as industrial sectors have been fabricated as shown in Figs. 6 and 7.

IV. Activities in Technology Promotion

A. Training Programme

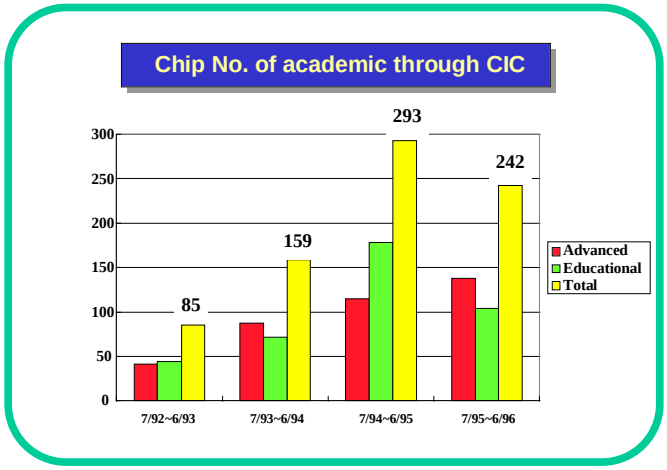

Fig. 6. Chip No. of the academics.

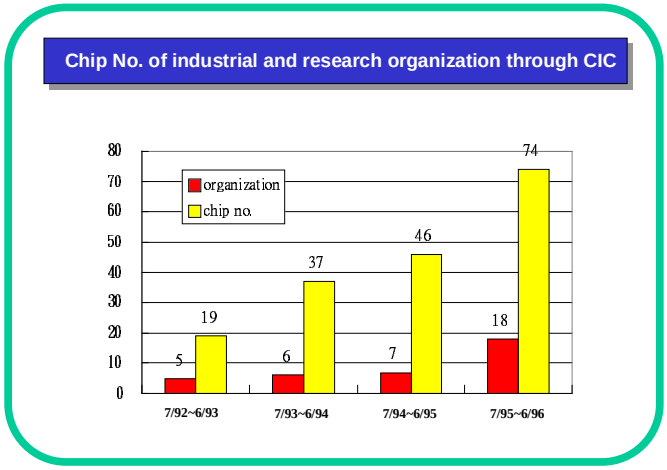

Fig. 7. Chip No. of industrial and research organization.

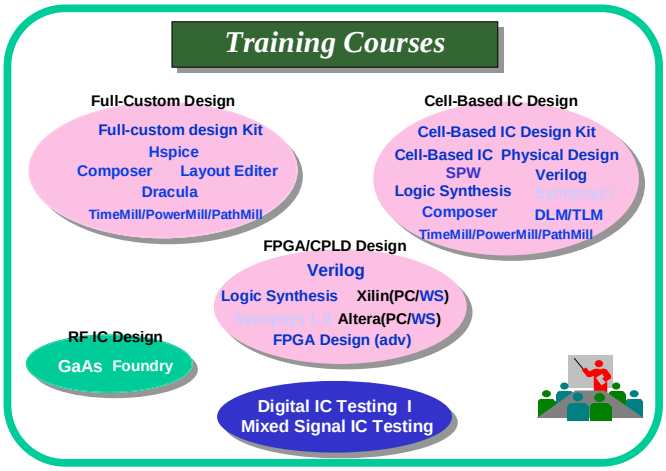

Fig. 8. Training courses grouped by CIC

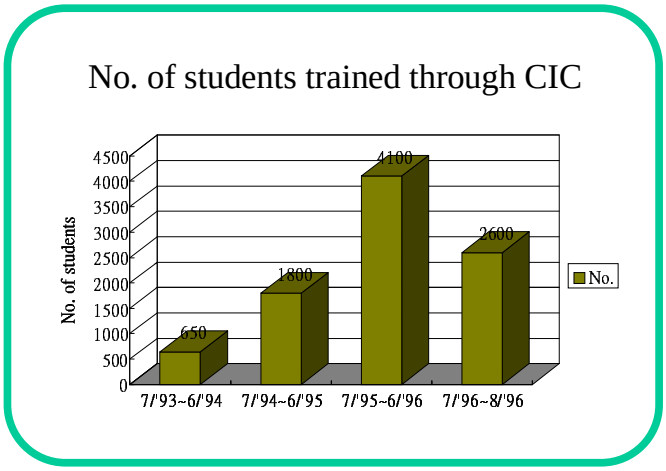

Fig. 9. No of students attending the training courses.

CIC runs various training courses and seminars covering the topics of full-custom IC design, cell-based IC design, FPGA design, RF IC design, IC testing, advanced course of CAD softwares, etc. Up to now, 22 courses (as shown in Fig. 8) have been opened. As shown in Fig. 9, 10000 engineers had been trained.

B. Network

In order to raise the design level and shorten the basic exploring time, the network in CIC is well-established. As shown in Fig. 10, CIC acts as a design consultant of the academics in Taiwan and provides the opportunities of experience exchange through the network.

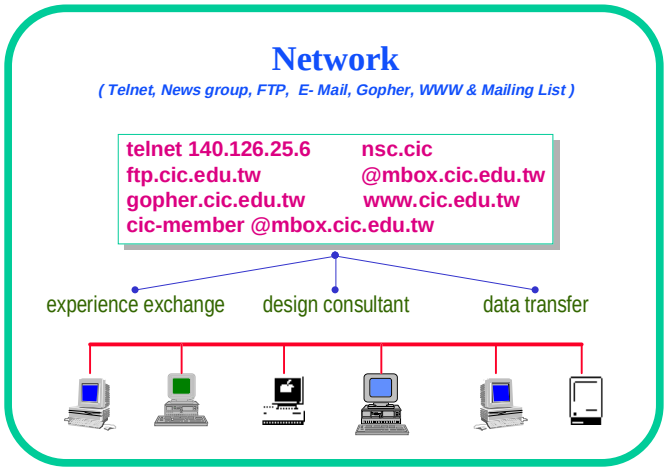

Fig. 10. Utilization of Network.

VI. Conclusion and Future Works

The coordinated action in MPC results in three aspect:

- sharing the mask, and thus increasing the number of chip manufacturing run;
- unifying the contact window with vender of EDA/IC manufacturer/tester, and thus relieving the labor of the academics; and
- transferring the innovated designs of universities, polytechnics and research institutions to industrial sectors for production.

With the mission of making R.O.C. a major player in the world hi-tech industries, CIC will continue to engage itself in those three activities. Moreover, CIC would encourage the R&D programmes led together by universities, polytechnics, research institutions, industrial sectors and the government.

Acknowledgment

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