Monte Carlo simulation for single electron circuits

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Abstract— In single electron circuits composed of small tunnel junctions, capacitances, and voltage sources, a tunneling electron can be described as a discrete charge due to stochastic nature of a tunneling event. We developed a *Monte Carlo* simulator for the numerical study of single electron circuits because no more conventional simulation methods based on Kirchhoff's laws can be applicable. The calculated dynamic operation of a quasi-CMOS inverter reveals that ultra small load capacitors give rise to large output voltage fluctuation during the logic operation. Future SET circuits should be designed with several electron logic rather than ultimate single electronic logic circuits in which a bit is represented with an electronic charge.

I. Introducton

During the last ten years a new physical phenomenon called Single Electron Tunneling (SET) has been extensively studied from the view point of solid state physics as well as its electronics circuit applications[1, 2]. It has been reported that the SET takes place at low temperatures in very small tunnel junctions implemented in electronic systems. The principle of the effect is based on an electric charging of junction capacitance as a result of electron tunneling through a junction.

Consider an electronic circuit in which a small voltage difference is applied to electrodes separated by an insulating barrier (∼2nm-thickness tunnel junction), as illustrated in Figure 1. Transfer of an electron through the barrier would result in electrostatic charging of the neighboring electrodes and hence in an increase of the electrostatic energy of the system by

$$\Delta E = \frac{Q^2}{2C} - \frac{(Q \mp e)^2}{2C} = -\frac{e(\mp Q + e/2)}{C}, \qquad (1)$$

where C is the effective capacitance between the neighboring electrodes and Q is the charge on the junction before the tunneling event. Forward and reverse tunnel events are designated with $-$ and $+$ signs, respectively. For $-e/2 < Q < e/2$ or the junction voltage of $-e/2C < V < e/2C$, the free energy of the system after the tunneling becomes higher than the initial state, thus the transition can be supressed over this range. This suppression is presently known as a Coulomb blockade of electron tunneling.

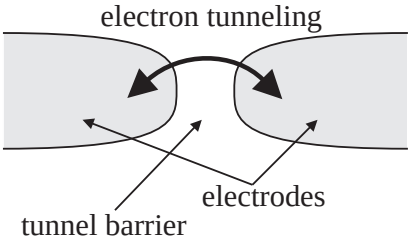

Fig. 1. The simplest system exhibiting the Coulomb blockade of tunneling.

There exist two major requirements to observe the Coulomb blockade effect. Firstly, tunnel resistance R_T of tunnel barrier must exceed the quantum resistance, $R_K = h/e^2 \sim 25.8\text{k}\Omega$. This condition ensures that quantum fluctuation with energy of $\sim h/RC$ is small compared with the charging energy of the order of $e^2/2C$. Secondly, the junction capacitance should be small enough to ensure that the electrostatic energy required to add a charge exceeds the thermal energy k_BT, where k_B is the Boltzmann's constant and T is operation temperature. In practice, typical capacitance of individual tunnel junctions fabricated with the state-of-the-art technology is the order of $\sim 10^{-18}$F where the charging energy , $e^2/2C$, overwhelms the thermal energy k_BT at room temperature. Thus, recent developments of nano fabrication technologies make it possible to observe the SET effect even at room temperature[6, 7].

Quite a few applications of the effect in analog and digital electronics are reported, such as capacitively or resistively coupled transistors[3], a turnstile device[4] and a pump circuit[5]. Although the physics on SET have been studied theoretically and experimentally during the past decade, only in the last few years SET circuit perfor-

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mances have been investigated using circuit simulators[8-12]. The objectives of this paper are two folds: (1) to introduce a basic algorithm of a Monte Carlo program suitable for SET circuit simulation and (2) to investigate electric characteristics inherent in a single electron circuit.

II. Calculation method of circuit performance

Conventional circuit simulations based on Kirchhoff's fundamental laws can be used only when an electronic charge is assumed to be continuous. In single electronic circuits where charge transfer due to SET is discrete and the event of the electron tunneling has stochastic nature, no conventional approach can be used for SET circuit simulation. Note that stochastic physical events have been well simulated with a Monte Carlo method. In our Monte Carlo simulation method[8] the tunneling rates Γ are the fundamental physical parameters to describe the frequency of electron tunneling events through tunnel junctions. This Monte Carlo method differs from conventional simulations in the following aspects; (1) node voltages change discretely after a tunnel event and (2) terminal voltages and charges on electrodes directly affect the tunneling rates, Γ.

Consider an arbitrary circuit consisting of metallic "islands" connected to each other and to external electrodes by tunnel junctions and/or normal capacitors. In the Monte Carlo simulation program, all the forward and reverse tunneling rates, Γ_i^+ and Γ_i^- in ith junction, are calculated. The tunnel interval $t_{i_{tun}}^{\pm}$ is evaluated for all tunnel junctions by using a generated random number r in the range of $0 \leq r \leq 1$ given by

$$t_{tun} = -\frac{1}{\Gamma_i^{+\text{ or }-}} \ln(r). \tag{2}$$

The minimum time interval $t_{min_{tun}}$ for electron tunneling is selected and compared with a time length $t_{\Delta V}$ in which an external applied voltage change exceeds a given threshold value. If $t_{min_{tun}} < t_{\Delta V}$, electron tunneling takes place at the tunnel junction. Then, $t_{min_{tun}}$ is added to total simulation time of the system. After the tunneling, data including the time, node voltages, and number of electrons in the nodes are updated. If $t_{min_{tun}} > t_{\Delta V}$, meaning the input voltage changes appreciably before the tunneling, the time of the system is advanced by $t_{\Delta V}$ without updating number of electrons in the nodes. The above processes are repeated until the time of the system exceeds a specified maximum time duration t_{end}. The flow chart of this procedure is shown in Figure 2.

III. Calculation of tunneling rate

The rate of an electron tunneling from a node to a neighboring one depends on the electrostatic energy difference ΔE and hence on the configuration of charges before and after a tunneling event. Based on a quasi-classical "orthodox" theory of single electron tunneling[1, 2], an electron is assumed to tunnel through one junction at a time. For the case of a low impedance environment the average tunneling rate Γ is given by

$$\Gamma = \frac{\Delta E}{e^2 R_T \left[1 - \exp(-\Delta E / k_B T)\right]}, \tag{3}$$

where R_T is tunnel resistance.

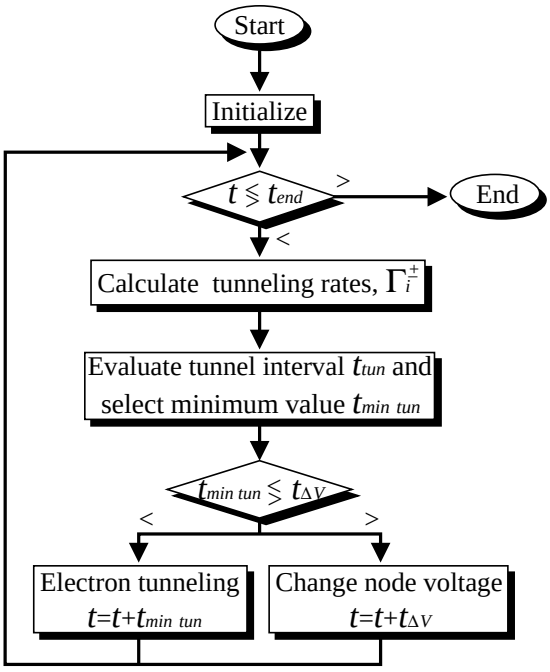

Fig. 2. Flow Chart of the Monte Carlo method.

We investigated SET circuits composed of capacitors and voltage sources. Based on the Thèvenin's theorem, any circuit to which a junction of interest is coupled is reduced to an equivalent capacitor C_{ext} together with a voltage source V[13] as shown in Figure 3. Suppose that before a tunneling, the net charge, ne, exists on an island. The energy change accompanying a transition from n to $n \pm 1$ can be given by

$$\begin{aligned} \Delta E^{n \to n \pm 1} &= \frac{e(\mp ne \mp C_{ext} V - e/2)}{C + C_{ext}} \\ &= \frac{e}{C}\left(|Q| - Q_c\right) \end{aligned} \tag{4}$$

where Q is the charge stored in the tunnel junction, and

$$Q_c = \frac{e}{2}\frac{C}{C + C_{ext}} \tag{5}$$

is a so-called critical charge of the junction[4].

Take a junction capacitor, C, connected to nodes i and j. A method to calculate the external equivalent capacitance, C_{ext} is described below. Assume that all voltage

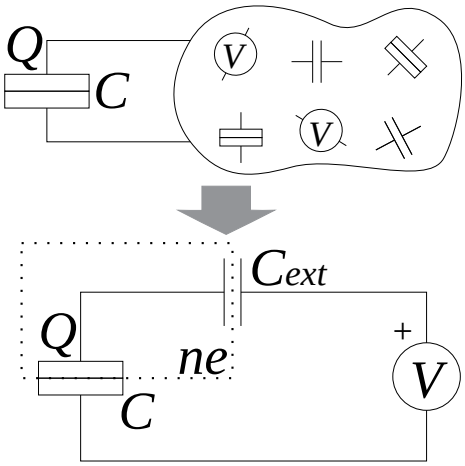

Fig. 3. Equivalent circuit representation of a single electronic circuit consisting of voltage sources and capacitances.

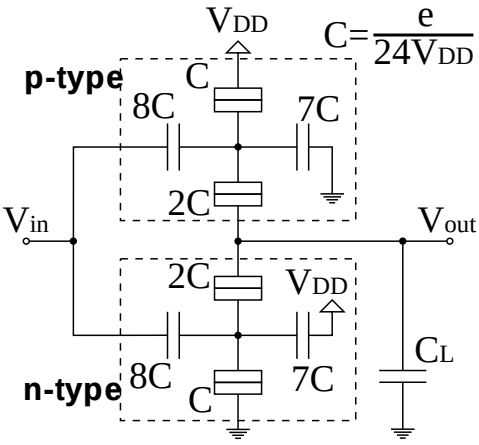

Fig. 4. Quasi-CMOS single electron inverter circuit[14].

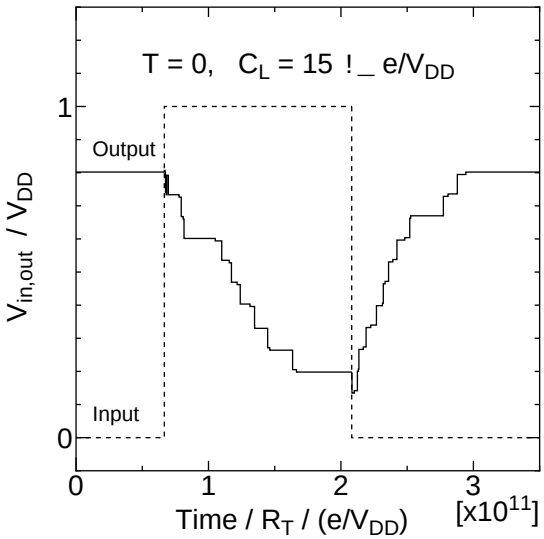

Fig. 5. Calculated output characteristics of the inverter circuit.

sources in the circuit are shorted and then a *virtual* voltage source, E, is connected between nodes i and j in parallel with the capacitor C. We solve a node equation of the circuit $\boldsymbol{CV} = \boldsymbol{Q}$ given by

$$\left[\begin{array}{ccc|c} C_{11} & \cdots & C_{1n} & -1 \\ \vdots & \ddots & \vdots & \\ C_{n1} & \cdots & C_{nn} & 1 \\ \hline 1 & & -1 & 0 \\ i & & j & \end{array}\right] \begin{array}{c} i \\ j \\ \\ \end{array} \left[\begin{array}{c} \boldsymbol{V} \\ \hline Q \end{array}\right] = \left[\begin{array}{c} 0 \\ \vdots \\ 0 \\ \hline E \end{array}\right] \tag{6}$$

$$C_{ij} = \begin{cases} i = j: & \text{sum of capacitances of all branches connected to node } i \\ i \neq j: & \text{negative of sum of capacitances of all branches connecting node } i \text{ and node } j \end{cases}$$

$\boldsymbol{V}$: potentials at each node
Q : charge on the ith node (= negative charge on the jth node)

As the effective capacitance between the nodes i and j becomes Q/E, the external capacitance C_{ext} is expressed as

$$C_{ext} = Q/E - C \tag{7}$$

IV. Results

Using our Monte Carlo simulator, we analyzed electrical characteristics of the basic inverter logic reported by Tucker[14] (Figure 4). The inverter circuit is composed of a quasi-n-MOSFET and a quasi-p-MOSFET, analogous to CMOS inverter circuit, both of which are made of two tunnel junctions and two normal capacitors. The bias capacitor of the quasi-n-MOSFET is connected to the positive supply voltage, while the bias capacitor of the quasi-p-MOSFET is grounded. In the quasi-CMOS inverter, the output voltage is proportional to the charge stored in the load capacitor C_L. We assume all the tunnel resistors have same resistance for simplicity.

Figure 5 shows the typical transient response of the quasi-CMOS inverter with $C_L = 15e/V_{DD}$. The abrupt changes of the calculated output characteristics represent the discreteness of electronic charge on the load capacitance. Note that fifteen electrons make it full logic swing at $C_L = 15e/V_{DD}$.

Figure 6 shows the calculated average gate delay time of the inverter as a function of the load capacitance. The large switching time variation is attributed to the discreteness of electronic charge: the decrease of C_L leads to the

large variation of the propagation delay time. An important conclusion is that the device performance degrades rapidly when C_L becomes less than $\sim 40e/V_{DD}$, in which about forty electrons represent one bit of information.

Figure 7 shows a cumulative distribution of propagation delay times at $C_L = 15e/V_{DD}$. The propagation delay time is defined as a time required for the output to exceed $0.8V_{DD}$ after providing a high-to-low input pulse. The calculated data points are found to be well fitted with a log-normal distribution function, solid curve. Based on the log-normal function, we estimated worst-case delay time at which an integrated circuit with 10^{10} inverters operating at an activity of 1% generates only one error for 10 year operation. Figure 8 shows the worst-case delay time as a function of load capacitance below which malfunction of the IC occurs. This is due to the fact that the switching time is too fast for some logic gates to catch up with it. Figure 8 also demonstrates that load capacitance should be large enough to avoid large delay time fluctuation such as 40 electrons for a bit representation. For example, clock rate should be of the order of 10 MHz to ensure proper operation of large scale integrated SET circuits with $R_T = 10^6\Omega$ and $e/V_{DD} = 10^{-17}$F.

V. Conclusion

We developed a Monte Carlo simulator to investigate dynamic characteristics of single electron circuits. The simulated results of the inverter circuit demonstrated that the switching time is significantly affected by a small fluctuation of the load capacitance for the case of the small load capacitor. In order to ensure proper logic operation, the load capacitance should be large enough to store at least 40 electrons because of drastic change of propagation delay time originating from small fluctuation of load capacitance. This means that "multi-electron" logics rather than ultimate "single-electron" logics is suitable for stable operation of SET logic circuits.

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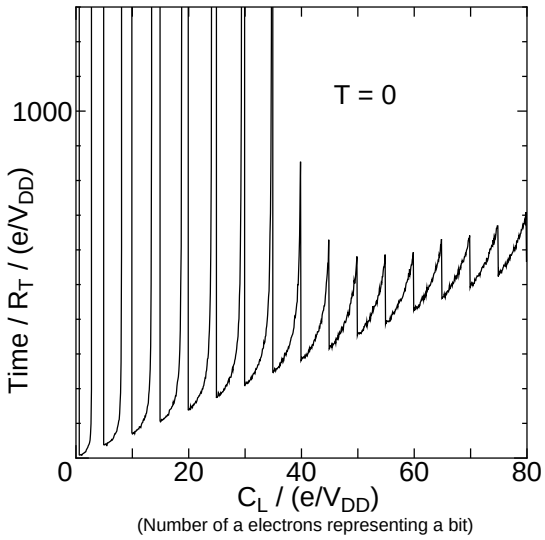
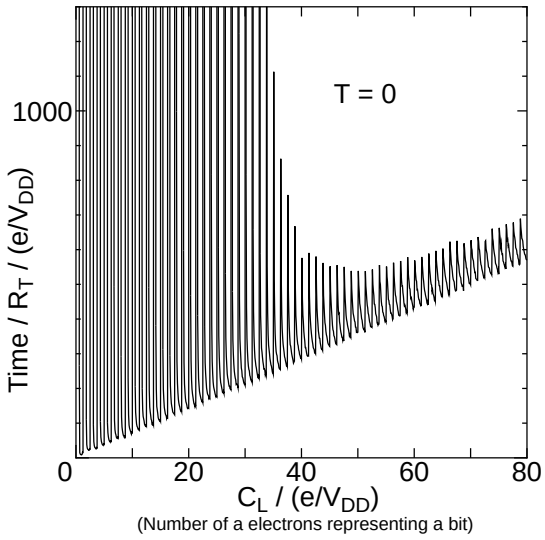


(a)



(b)

Fig. 6. Switching time as a function of the load capacitance C_L. Input voltage is switched (a) from 0 to 1, (b) from 1 to 0.

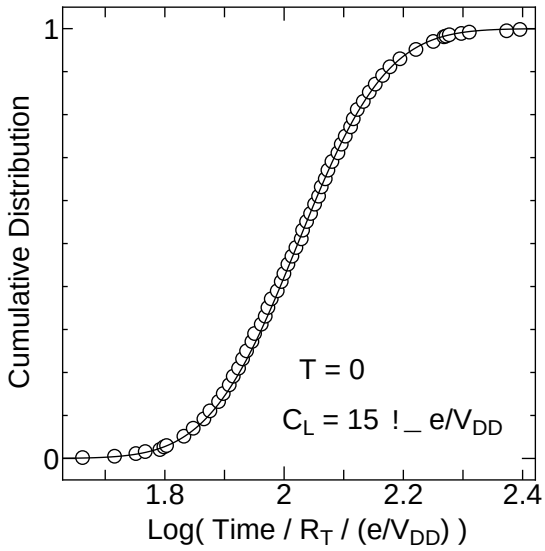


Fig. 7. Cumulative distribution of calculated propagation delay times: open circles. Solid curve represents a log-normal function.

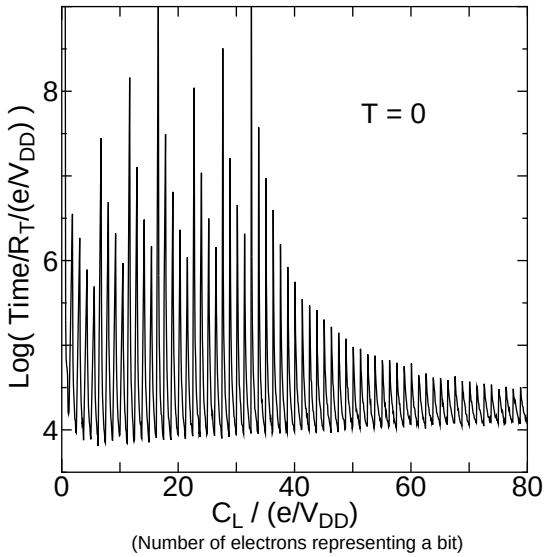


Fig. 8. The worst-case delay time as a function of load capacitance below which malfunction occurs.